UNIVERSIDAD DE SEVILLA
Departamento de Electrónica y Electromagnetismo

UNIVERSIDAD DE LA REPÚBLICA
Instituto de Ingeniería Eléctrica

An All-Inversion-Region g_m/I_D Based Design Methodology for Radiofrequency Blocks in CMOS Nanometer Technologies

Memoria presentada por

RAFAELLA FIORELLI MARTEGANI

para optar al grado de Doctora
por la Universidad de Sevilla y la Universidad de la República

Octubre, 2011

An All-Inversion-Region g_m/I_D Based Design Methodology for Radiofrequency Blocks in CMOS Nanometer Technologies

Memoria presentada por

RAFAELLA FIORELLI MARTEGANI

para optar al grado de Doctora
por la Universidad de Sevilla y la Universidad de la República

Octubre, 2011

Dirigida por

Dr. Eduardo Peralías Macías
Científico Titular del CSIC
IMSE-CNM, España

Dr. Fernando Silveira Noguerol
Profesor Titular - Universidad
de la República, Uruguay

Tutores :

Prof. Adoración Rueda Rueda
Catedrática de la Universidad de Sevilla, España
Prof. Fernando Silveira Noguerol
Profesor Titular -Universidad de la República, Uruguay

Departamento de Electrónica y Electromagnetismo
Universidad de Sevilla
Instituto de Ingeniería Eléctrica
Universidad de la República

A mi familia y a Juan.

Esta tesis fue realizada en Régimen de Cotutela entre la Universidad de Sevilla, España y la Universidad de la República, Uruguay, en el marco del convenio firmado por estas universidades y es reconocida por ambas Universidades para los respectivos programas de Doctorado.

Agradecimientos

En primer lugar agradezco a mis directores de tesis Eduardo Peralías y Fernando Silveira, y mi tutora, Adoración Rueda, que sin su tiempo, dedicación e invalorable ayuda este trabajo no hubiera llegado a buen puerto. Quiero también agradecer a José Luis Huertas por su apoyo y ayuda durante estos años de trabajo en el IMSE.

Me gustaría agradecer aquí a todos y cada uno de mis compañeros y amigos tanto de mi grupo de investigación como del IMSE en general, ellos han hecho que estos años hayan sido un tiempo de enriquecimiento profesional y personal. A la distancia, también quiero expresar mis agradecimientos a mis compañeros del Grupo de Microelectrónica y del Instituto de Ingeniería Eléctrica de la Universidad de la República.

Mi querida familia, mis amigas y amigos y Juan saben, más que nadie, lo feliz que me siento de haber llegado a esta etapa de mi carrera profesional y los obstáculos y problemas que han surgido en este tiempo y que entre todos estamos intentando superarlos. Sin su inmenso cariño y apoyo incondicional, yo no estaría aquí, ahora.

Finalmente, han sido muchas instituciones que han apoyado este trabajo técnico y que deseo listar aquí. Sin lugar a dudas quiero mencionar al Instituto de Microelectrónica de Sevilla (IMSE-CNM) del CSIC-España, la Universidad de Sevilla-España y la Universidad de la República-Uruguay, por su apoyo técnico, logístico, y financiero, al Ministerio de Asuntos Exteriores y de Cooperación por la financiación de mi beca doctoral MAE-AECID durante estos tres años y al servicio de fabricación de MOSIS. Por otra parte agradezco los siguientes proyectos que han financiado en parte este trabajo de investigación: 1) el gobierno español y los fondos FEDER a través de los proyectos SR2 (TSI-020400-2010-55/Catrene2A105SR2, TSI-020400-2008-71/MEDEA+2A105), TOETS (CATRENE CT302) y TEST(TEC2007-68072/MIC), 2) el gobierno andaluz con el proyecto ACATEX (P09-TIC-5386), 3) el gobierno uruguayo con los proyectos ANII FCE 2007/501 y PDT 63/361 y 4) el proyecto de cooperación bilateral CSIC-UR 2009UY0019.

Contents

Resumen

ESTA TESIS TRATA del diseño, en tecnologías nanométricas CMOS, de bloques analógicos para aplicaciones de RF, en el que se ha incorporado como base la completa exploración de todas las posibles regiones de inversión en las cuales el transistor puede ser polarizado. La herramienta fundamental ha sido el uso sistemático de la técnica g_m/I_D sobre los transistores y la descripción del comportamiento real de todos los dispositivos mediante modelos semi-empíricos. Dos circuitos han sido estudiados cuidadosamente en este trabajo: el amplificador de bajo ruido (o LNA) y el oscilador controlado por tensión (o VCO). Para cada uno de estos circuitos, se han elaborado y plasmado en flujos de diseño varias estrategias de diseño óptimo. Mediante el análisis de las variaciones de las características de los circuitos estudiados, como figura de ruido, ganancia en potencia, consumo, en función del parámetro g_m/I_D de cada transistor, se puede seleccionar la región de inversión óptima, obteniéndose un razonable coste en el diseño de estos bloques, a partir de varias herramientas de cálculo y optimización que se han desarrollado específicamente. Basándonos en las especificaciones de los estándares de comunicación de RF de bajo consumo, se ha diseñado un conjunto de estos circuitos, donde se demuestra la efectividad del método implementado. Dos procesos nanométricos fueron utilizados en las respectivas implementaciones. Los resultados obtenidos mediante simulaciones eléctricas y medidas concuerdan razonablemente con los obtenidos con las herramientas de cálculo. Por último, esta metodología se ha utilizado tanto en el estudio previo como en el diseño final de algunos bloques de RF de un transceptor ZigBee de 2.4 GHz.

Abstract

THIS THESIS DEALS with the design, in CMOS nanometric technologies, of analog blocks for RF applications, based on the complete exploration of all-inversion-regions in which the MOS transistor is biased. The fundamental tool has been the systematic use of the MOS transistors g_m/I_D technique and the description of the real behavior of all devices by means of semi-empirical models. In this work, two circuits have been carefully studied: the low noise amplifier (or LNA) and the voltage controlled oscillator (or VCO). For each of these circuits, several optimum design strategies have been elaborated and expressed in design flows. Through the analysis of the variations of the studied circuits features, as noise figure, power gain, consumption, as function of the parameter g_m/I_D of each transistor, it is possible to select the optimum MOS transistor inversion region. This way it is obtained a reasonable design cost for these blocks, starting from the computation and specifically developed optimization tools. Basing our designs on the low power RF communication standard specifications, a set of these circuits have been designed, where it is shown the effectiveness of the developed method. Two nanometer process were used for the referred circuits implementation. The results obtained from electrical simulations and measurements agree with the ones collected with the computational tools. Finally, this methodology has been used both in previous studies and final design of some of the RF blocks of a 2.4 GHz ZigBee transceiver.

CHAPTER 1
Introduction

WIRELESS APPLICATIONS in areas as diverse as medicine, entertainment or environment have originated a wide spectrum of wireless standards which are reflected in diverse system specifications. The prompt translation of these characteristics to a final design, required due to the shrinking time-to-market, is a big challenge. Considering those wireless applications with emphasis in low-power consumption, their increasing demand and the competitive market obliges the designer to push the technologies to their limits and, at the same time, to reduce costs. This cost reduction is done by means of utilizing CMOS technologies which, since a few years ago, are sufficiently mature to be applied in radiofrequency applications. As other dominant RF technologies, as GaAs, have higher performances than CMOS, to achieve these challenging specifications with this technology, an optimization is needed in each block of the system, especially when talking about power consumption, noise, linearity and silicon area. RF designers, as never before, need reliable CMOS optimization tools helping them from the beginning of the design process. It is specially appropriated when using power-consumption demanding RF standards but relaxed in other electrical requirements e.g. in terms of channel bandwidth or noise and frequency synthesizer spectral purity, as in the case of ZigBee standard (IEEE 802.15.4) and low-energy Bluetooth (IEEE 802.15.1). The typical applications of the mentioned standards include wireless sensor networks, industrial and personal uses running on just "button" batteries, or medical applications.

Power consumption constrains the design of the transceiver and forces to assign carefully the power budget of each block of the chain. The election of the circuit driving current strongly influences the circuit noise as well as its power gain or its linearity, to name typical analog circuit electrical characteristics. The well known trade-off between power and the inherent noise of RF blocks is especially noticeable, as in voltage controlled oscillators, low noise amplifiers or mixers. To exemplify, a very low-noise application should accept high power consumption, whereas a very low-power design would need to manage higher noise values. Especially when nanometer technologies are involved, to take advantage of such compromise, the RF designer needs a deep and accurate knowledge of the circuit behavior as well as of the electrical devices features included in the block, in order to reach the goal of an optimized design. In particular, the use of opti-

mization techniques applied before electrical simulation is an appealing alternative, as presented in [Deng 11, Nieu 09, Nguy 04, Bara 10, Shae 97, Andr 01, Belo 06, Jans 02, Ramo 05, Tang 08, Sanc 10]. Some of these methodologies are somewhat quite "circuit specific" and cannot be generalized to other blocks.

The existent trade-off between power consumption and noise or power gain circuit characteristics are strongly determined by the active element: the MOS transistor (or MOST). These circuit features change as function of the inversion region in which the MOS transistor is biased. The MOST used in analog and radiofrequency has been traditionally biased in strong inversion region (SI). This region is characterized by high power consumption as well as high MOST transition frequencies due to the small sizing of the MOST. In this zone the MOST gate-source voltage V_{GS} is well above the threshold voltage V_T, also called the above-threshold region. But in the MOST other two inversion regions can be distinguished: the weak inversion region (WI) -or sub-threshold region-is the zone where V_{GS} is well below V_T; and the moderate inversion region (MI) which is in the midst of weak and strong inversion, approximately "around" threshold. These last two regions consume much less power but reach lower transition frequencies due to the increment in MOST sizes.

In low-power analog circuits, working low and medium frequencies, it is crucial the use of the MOST in moderate and weak inversion regions, taking advantage of the nanometer technologies proliferating nowadays. Hundred of published works, studying both the MOST device and the circuits in which it is embedded, guarantee the good performance of these regions, usually discarded or feared to be used fifteen years ago. First works ares that of Koomen [Koom 73] or the one of Vittoz and Fellrath [Vitt 77], and, to give some examples, it would continue with the following list of publications, probably incomplete, of the most important works in this area [Vitt 79, Vitt 85, Cast 85, Andr 91, Malo 95, Heim 95, Silv 96, Cunh 98, Tsiv 00, Lina 03, Harr 03, DJCo 04, Rodr 04, Geor 05, Shen 08]. In the two research groups in which this thesis has been developed, several contributions have been presented to help consolidating the work on these regions as useful and reliable ones, as it can be appreciated in the papers of [Silv 96, Silv 00, Acos 02, Agui 03, Silv 04, Rodr 04, Yufe 05, Arna 06, Agui 08, Barb 06, Vill 10].

Nevertheless, when working in radiofrequency, the MOS transistor has been traditionally biased in strong inversion, as it is shown in [Wu 98, Rofo 96, Wata 99]. It is because in this region the transistor has small sizes and drives higher currents than in moderate or weak inversion. This leads to a reduction of parasitic capacitances and an increment in the transconductance. As the MOST transition frequency f_T is proportional to the transconductance and to the inverse of its parasitic capacitance, the maximum f_T increases in strong inversion region. However, this increment in the maximum frequency of operation is obtained at the expense of very low ratios between transconductance and bias current (below 5 V^{-1} in-

stead of the 38 V^{-1} achievable with a bipolar transistor at ambient temperature). So, moving from strong inversion through weak inversion implies a considerable current reduction, but on the opposite, an increment in the parasitic capacitances and hence a reduction in the f_T. For example, for sub-micrometer technologies, radiofrequency design in moderate is limited up to one gigahertz [Barb 06].

The tremendous channel length reduction below 100 nm, and the improvement in passive components, i.e. inductors, capacitors and resistors, opens the path to feasible implementations in radiofrequency in moderate/weak inversion. Since a few years ago it is possible the use of CMOS technology without increasing too much the power consumption and even reduce it by working in moderate and weak inversion regions in the range of several gigahertz. This can be achieved even considering the MOS transistor working below the quasi-static limit of one tenth of f_T (as Tsividis presents in [Tsiv 00], p. 492) and therefore greatly simplifying the circuit analysis.

Regarding the use of on-chip inductors, the availability of reasonable high-quality-factor coils opens up new possibilities in the optimization field, as Ramos clearly presents in [Ramo 05]. Non considering the real features of the different inductors embedded in the design leads to absolutely under-optimized circuits and even non-working blocks.

Many RF implementation examples working in moderate and weak inversion are found in literature. Porret et al. [Porr 01] and Melly et al. [Mell 01] presented the design of a receiver and a transmitter, respectively, for 433 MHz in CMOS, working in moderate inversion. Ramos et al. [Ramo 04] showed the design of an LNA in 90-nm technology for 900 MHz in moderate/weak inversion. In [Fior 09, Barb 06] we utilized the moderate inversion to implement an RF amplifier and a VCO at 900MHz. Shameli and Heydari [Sham 06] designed a CMOS 950-MHz LNA in moderate inversion. Lee and Mohammadi designed a 2.6-GHz VCO [Lee 07] and a 3-GHz LNA [Lee 06] in weak inversion in CMOS. Do et al. designed a mixer [Do 09] and an LNA [Do 08] in the subthreshold region for 2.4 GHz. Jhon et al. [Jhon 09] designed a 0.7-V, 2.4-GHz LNA in deep weak inversion. To provide a final example, Valdes-Garcia et al. [Vald 08] designed a broadband CMOS amplitude detector for on-chip RF measurement, with some blocks working in weak inversion. These works, among many others show how, in the last decade, the design in moderate and weak inversion in CMOS in RF became consolidated and the observed tendency is that the application of these approximations will continuously grow. However, there is a lack of published design methodologies which cover and systematically study all the MOS transistor inversion regions and provide a way for exploiting the involved trade-offs, going farther than just showing the feasibility of a particular design.

This thesis deals with the design in nanometer CMOS technologies of analog blocks for RF applications, exploring completely all-inversion regions in which the MOS transistor can be biased. The fundamental tool to achieve this objective is the systematic use of the transconductance-to-current-ratio, g_m/I_D, technique of the MOS transistor, presented in the work of Silveira, Flandre and Jespers in 1996 [Silv 96] and the description of the real behaviour of all the devices by means of semi-empirical models. The g_m/I_D ratio versus the normalized current $i = I_D/(W/L)$ [Cunh 98, Enz 06, Galu 99], is an intrinsic MOS characteristic which indicates the inversion level of the transistor (i.e. strong, moderate or weak inversion). Biasing the transistor in strong inversion means low g_m/I_D values while working in weak inversion is translated to high g_m/I_D figures.

The g_m/I_D ratio properties make it suitable to be the fundamental tool of our design method [Jesp 10]. Firstly, its value gives a direct indication of the inversion region. Secondly, its variation is constrained to a very small range, efficiently covered with a grid of some tens of values of g_m/I_D (e.g. from 1 V^{-1} to 30 V^{-1} in nanometer bulk pMOS). Finally, by using the circuit expressions and sweeping g_m/I_D -which implicitly or explicitly appears in them-, we achieve a detailed study of the circuit characteristics as function of the inversion region. The analysis of the variations of each circuit's characteristics, as noise figure, power gain or power consumption, as function the g_m/I_D parameter helps us to select the MOST optimum inversion region to have a design cost equilibrated to the concrete RF application [Flan 97, Bink 08, Agui 08, Gira 06].

As it will be clear afterwards in this dissertation, the proposed approach allows to reduce power consumption for a given set of specifications. The basic idea is to reach the circuit requirements without an unnecessary improvement in any of its characteristics (i.e. phase noise in oscillators or noise figure in low noise amplifiers) because it generally entails a waste of power. In this work will prove that in moderate inversion, where low power consumption is achieved, we obtain those trade-offs. This last fact highlights the importance of having a design methodology which covers the complete range of the inversion zones.

The characteristics of the active and passive devices substantially modify the circuits behaviour, meaning that a good modeling of the technology involved in the design is necessary. Having an incorrect modeling would lead to a substantial difference between the circuit features in the design level and after electrical simulation. To describe the MOS transistor and the passive devices three type of models can be classified:

1. Analytical models: equation or topology physical-based models. These models provide relations between basic electrical magnitudes (currents or voltages) which parameters are obtained from fitting procedures from measured data.

2. Empirical models: manifolds fitted from measurements or simply look-up tables (LUTs), which parameters are non-physically based.

3. Semi-empirical models (or semi-analytical models): are the models that are neither analytical nor empirical. We divide them into two sub-types:

   (a) Analytical models which parameters are in LUTs and depend on primary electrical magnitudes.

   (b) Empirical models which data are obtained from analytical models, e.g. LUTs obtained from electrical simulations (either from fundamental semiconductor equations in three dimensions or electromagnetic equations of the passive devices; or from analytical models)

To mention some examples of analytical models for the MOST used nowadays we have BSIM [BSIM 08], PSP [Gild 06], EKV [Enz 06] or ACM [Cunh 98]. In this work, either for MOS transistors and passive devices, we use the two kind of semi-empirical models previously defined.

Two core circuits are thoughtfully studied in this dissertation, the LNA and the VCO. We elaborate optimum design strategies for each of them, which are expressed in design flows. These circuits have the noise as a fundamental feature: the phase noise for the oscillators and the noise figure for low noise amplifiers. Therefore the noise characteristics of the devices, in special of the MOST have been reviewed here in terms of the MOST inversion regions. This is the case of the drain noise current which generally is a large percentage of the total MOST noise; its parameters have been extracted as function of the g_m/I_D, and used in the design flow, whenever is proven to be necessary. Up to what we know, it is the first time flicker noise has been analytically included in the LNA noise figure calculations; we observe its effect in the noise for moderate and strong inversion regions. For the VCOs, phase noise models suitable for all-inversion regions are presented for both white noise and flicker noise regions.

Optimization and evaluation tools are developed for the circuits design by means of Matlab computational routines that implement the design flows of the LNAs or VCOs blocks and embed the devices LUTs. The electrical simulator, Spectre RF, is used to verify the methodology.

Regarding the technologies used in this thesis, to implement the designed blocks two nanometric processes are utilized. For the design and implementation of the LNAs, it is utilized the TSMC 90nm 1P9M CMOS technology, called TECH1 from now on. This process includes analog and RF transistors for 1.2 V and 2.5 V supply voltages; parametrized library cells for the generation of a wide spectrum of inductors (single-ended and symmetrical), capacitors and resistors, and also includes analog and RF I/O pads. For the design and implementation of the VCOs, the IBM 90nm 1P8M CMOS technology is used, called TECH2. This process has

1.2 V RF transistors and 1.8 V I/O transistors also RF modeled, is also has passive parametrized library cells (only symmetrical inductors are provided), a good ESD cell library, however no pre-designed I/O pads are supported which forces us to design them. Both technologies reach transition frequencies above 100 GHz, enabling us to work quasi-statically at frequencies below 10 GHz.

In the following section, the design methodology is presented, providing a description of its steps.

1.1 Design methodology developed in this thesis

In this thesis we develop a design methodology for RF blocks which gives a simple and systematic way to size MOS transistors and passive components and permits to visualize the compromises involved in the design of an RF block. The technology data are initially collected and subsequently used in the proposed design flows as LUTs. These flows use the real characteristics of all the devices presented in the circuits as optimization variables, especially considering the all-inversion-regions of the MOS transistor.

The basic idea is that each g_m/I_D value is one to one related with the normalized current i value, as Fig. 1.1 shows. With this approach, we consider a range of g_m/I_D, i.e. between 3 V^{-1} (deep strong inversion) and 25 V^{-1} (weak inversion), and the drain current I_D varying between two limit values, $I_{D,min}$ and $I_{D,max}$. Then for each possible pair (g_m/I_D, I_D), the normalized current i, the transconductance g_m and the transistor aspect ratio W/L are deduced. As in this case the transistor length L is set to the technological minimum to reach the highest f_T, the width W is solved.

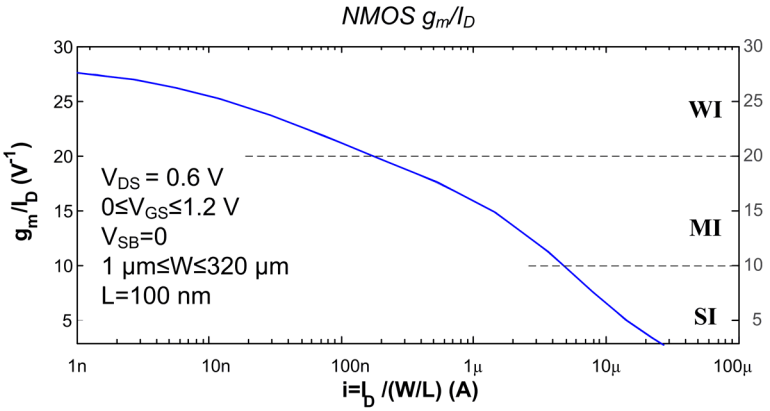


Figure 1.1: *g_m/I_D vs. i for nMOS transistors.*

A hypothesis of our RF design methodology is the operation of the MOS transistor device in the quasi-static zone, i.e. the RF working frequency f_0 is at MOS transistor one tenth of the transition frequency. Due to this hypothesis, we use the five-capacitance MOS transistor model (C_{gs}, C_{gd}, C_{gb}, C_{bs} and C_{bd}) [Tsiv 00].

Semi-empirical models for the MOS transistor and passive devices, obtained from electrical simulations are chosen to model the technology. Some element characteristics are described with analytical models, which parameters are in LUTs, as the power spectral density (psd) of the MOS transistor noise sources. For the rest, empirical models which data are obtained from analytical models are used, by means of LUTs.

Another important consideration taken throughout this dissertation is the implementation of the design methodology in the process typical corner, leaving the study of other corners for the circuit's electrical simulations. It means that the devices models used in the design routines are the semi-empirical models considering only the typical corners data. Nevertheless, corners simulations are presented to know beforehand the MOS transistor corner-sensitive device characteristics.

Four steps have to be followed to apply our design methodology for an RF block [Fior 11a, Fior 11c, Fior 12, Fior 11b]:

1. **MOS transistor semi-empirical modeling**

   Low-frequency behavior of MOS transistor has to be captured in curves, LUTs or expressions. It is necessary to measure or simulate the MOS characteristics (transconductance g_m, drain-source conductance g_{ds}, drain current I_D, quasistatic normalized intrinsic capacitances C'_{ij}, with $ij = \{gs, gd, gb, bd, bs\}$) for a small set of transistor sizes and for all-inversion regions (for example, sweeping the gate-source voltage for a fixed drain-source voltage, and measure the drain current I_D) in order to generate the curves g_m/I_D versus i and g_{ds}/I_D, C'_{ij} versus g_m/I_D and overdrive voltage versus g_m/I_D. The parameters corresponding to the noise models should be also extracted. In this work the extraction of the characteristics mentioned in this item is done by electrical simulation with the parameters provided by the foundry.

2. **Passive semi-empirical modeling**

   Parasitic parameters extraction of components have to be expressed in LUTs, for a working frequency, for inductors, capacitors and resistors. The objective is to have one-to-one relations to get the best feasible device from its nominal value. The qualifier "best device" could be in the sense of, for example, the best quality factor or, the lowest series parasitic resistance, for a given value of inductance.

3. **Signal and noise modeling**

   RF block core characteristics are modeled. When necessary, perform the equations modifications to link with the device characteristics described in the methodology steps 1) and 2).

4. **Design Flow**

   Create a simple and systematic design flow where the relations between the block equations, the extracted parameters and the necessary decisions are properly organized, all intended to fulfill the particular specifications of the block and technological process constraints.

Lets exemplify these ideas with a circuit studied in this work: an LC-VCO. The first two items are themselves independent of the circuit used, they characterize the technology. However, the knowledge of *a priori* circuit operating conditions could reduce the number of simulations. For example, if we use a differential LC-tank VCO, the drain voltages of the nMOS and pMOS are roughly around half the supply voltage, so there is no need to study these transistors for a wide drain voltage range. The same comments serve for passive devices: e.g. for a differential LC-tank VCO, the inductor must be a differential one, so the characterization should be done considering this fact.

In the third item, an analytical description of the circuit is needed. Considering the VCO, oscillation frequency, oscillation condition, phase noise, output voltage amplitude, among others features should be functions of the MOS transistor features, the drain current and passive devices characteristics, to provide an analytical VCO representation.

The fourth item picks the circuit required specifications (i.e.: minimum phase noise, minimum output voltage amplitude), the MOS transistor data versus the g_m/I_D ratio, the passive features (e.g. inductor parasitic resistance versus inductance) and the block equations and reorders them setting out a coherent design flow, always starting from a given g_m/I_D ratio. The optimization is done in this step, and as it uses real technology data as optimization variables, the final results match very well the circuit electrical simulations.

1.2 Thesis Objectives

The general objective of the thesis is the design of analog blocks for RF applications in nanometer technologies, based on the fully exploration of the MOS transistor all-inversion regions.

The specific objectives are the following

1. Study the feasibility of applying the g_m/I_D ratio as a basic design tool in RF circuits.

2. Validate the use of semi-empirical models extracted from electrical simulation for all the circuit devices: MOS transistor and passive components. Verify the utility of the simple models utilized for passive components.

3. Examine the semi-empirical models of MOS transistor noise for all-inversion regions, in particular the drain current noise and the flicker noise. Study how essential is the inclusion of this model in the accurateness of the final results.

4. Develop systematic design flows for the specific RF circuits. The obtained designs should be sized with enough precision in order to need only slight modifications in the final step of the electrical simulations due to layout parasitics.

5. Specifically for LNA and LC-VCO: prove that the moderate inversion is optimum in the sense of minimize the noise for a limited power consumption.

6. Specifically for LC-VCO, obtain a phase noise model valid for all-inversion regions.

7. Implement in nanometer technologies some of the designs obtained with the methodology in moderate/weak regions to corroborate the methodology.

1.3 Thesis Organization

This dissertation is organized as follows.

Chapter 1 presents the background of the thesis and introduces the main ideas of this dissertation. It also presents an overview of the thesis design methodology and its principal objectives. Finally, the organization of the dissertation is sketched.

Chapter 2 details the approaches utilized throughout the methodology to describe the MOS transistor and the passive devices and to obtain the database used in each circuit design flow (semi-empirical models). In particular, a concise description of the MOS transistor in all-inversion regions considering the MOS transistor g_m/I_D ratio is provided. In addition, the modeling schemes of inductors, capacitors and resistors are provided, as well as graphical examples of their parasitics.

Chapter 3 presents the design methodology of the differential cross-coupled LC-VCO architecture The corresponding set of equations for signal and phase noise is derived and two design flows for phase noise minimization are deduced considering a simple and a general approach. This methodology is validated by means of a set of design points biased in different inversion regions obtained with computational routines and electrically simulated with SpectreRF from Cadence. One of these design points has been fabricated, and its measurements presented.

Chapter 4 studies the design methodology of two LNA architectures: the common source LNA (or CS-LNA) and the common gate LNA (or CG-LNA). For both architectures their set of equations for signal and noise figure and the corresponding design flows are provided, which focus on minimizing the noise figure. As done with the LC-VCO of Chapter 3, the methodology is validated by comparing the computational data with the electrical simulated results of SpectreRF. The measurements of a fabricated CS-LNA are displayed to provide more insight to the method.

Chapter 5 presents the implementation of RF-block designs for a ZigBee transceiver where the developed design methodology (or part of it) is used. It is shown the design of a single-ended input front-end which utilizes a CS-LNA, designed under the developed design methodology. Also, the design of a demonstrator of an RF test methodology is presented, which includes a modified version of the single-ended CS-LNA. Then, a power amplifier design, based on a modified version of the design methodology proposed in this dissertation for large-signal, is included. Finally, an overview of the design of the analog front-end of a ZigBee transceiver, designed by the whole research group, is introduced.

Chapter 6 summarizes the main conclusions of this thesis and lists the proposed future lines of work.

Chapter 7 presents the conclusions of Chapter 6 in Spanish.

CHAPTER 2

Modeling of nanometer RF CMOS processes

THE RADIOFREQUENCY DESIGN METHODOLOGY presented in Chapter 1 is based on the characteristics of the elements used in the RF circuits. The basic component of every RF active circuit is the MOS transistor. In nanometer technologies, MOST channel length reduction and other technology limitations generate non-idealities in all-inversion regions. These non-idealities, already included in analytical models as EKV [Enz 06], ACM [Galu 99] or PSP [Gild 06], pose a problem when a quick MOST model in all-inversion regions wants to be obtained. Unfortunately, the simple model provided by analytical models in micrometer technologies cannot be used for the newest RF CMOS processes. This approach can be substituted by the complex set of equations provided by analytical models or semi-empirical models as has been already discussed in Chapter 1. In any case, these models need either simulations or measurements of MOST samples to obtain or the parameters of the equation set or the dataset.

Accordingly, this chapter deeply analyzes the MOST features used throughout this dissertation. We particularly discuss the utilization of semi-empirical models or analytical compact models, justifying the election of the former as the one used in this thesis. The operation and modeling of the MOS transistor in all-inversion regions is included in the study, considering particularly one of the basic tools of this thesis: the g_m/I_D ratio versus the normalized drain current i. We study the MOST output conductance over drain current ratio, g_{ds}/I_D, the normalized quasi-static intrinsic capacitances, the over-drive voltage $V_{OD} = V_{GS} - V_T$, and the noise parameters as function of the g_m/I_D ratio. The validity of describing the MOST characteristics considering a small set of transistor widths is specially emphasized. MOST data features are collected using the typical corner. To know beforehand which MOST characteristics have more sensitivity to fast and slow corners, a brief study is also presented.

Passive elements, as inductors or capacitors, are undoubtedly basic components of monolithic RF designs and their performances substantially affect the optimization derived in this thesis. Luckily, passive devices have improved with technology progresses, reducing their parasitics, especially when concerning inductors. These

parasitics affect RF circuits features as noise, gain or consumption, hence their quantification is compulsory needed as well as their mandatory inclusion in the optimization process.

In this dissertation inductors, capacitors (and varactors) and resistors available in the fabrication process are modeled and studied. The benefits of modeling them by analytical or by semi-empirical models as well as the reason of the election of the later one in this thesis are briefly discussed . The three of them are deeply studied both for the typical condition and for the process corners, to capture their variability.

Despite two 90nm CMOS RF technologies are used throughout this work, named TECH1 and TECH2, this chapter only presents the results and graphs of TECH1 in order to homogenize and clarify the information. Some fundamental data of TECH2 are included in Appendix 2.C. Unless otherwise stated, the transistors used are set to the minimum length of the technology, i.e. 100 nm, in order to achieve the highest transition frequency.

This chapter is organized as follows. Section 2.1 introduces the MOS transistor operation as well as the analytical and semi-empirical modeling discussion. Section 2.2 analyzes our chosen MOST semi-empirical model and the low-frequency MOST characteristics for all-inversion regions. This chapter finalizes presenting Section 2.3, where the passive components semi-empirical models used throughout this thesis.

2.1 MOS transistor operation and modeling

To systematically develop optimization methodologies for RF blocks, considering all-inversion regions of the MOS transistor, we need a deep comprehension of the MOS behavior as well as accurate MOS transistor models. This section presents this study and introduces the g_m/I_D ratio, one of the fundamental tools of this work.

Initially, a theoretical analysis of the the MOST behavior in its different operation regions is presented, deducing the g_m/I_D ratio versus the drain current I_D and versus the normalized current i. As this work is focused on radio-frequency analog blocks, a special discussion regarding the behavior of the MOS transition frequency, f_T, for all the regions of operation is included. Then, the effect of the MOST g_{ds} conductance as well as the g_{ds}/I_D ratio versus g_m/I_D is considered here. Subsequently, the study of the quasi-static five-intrinsic-capacitances scheme as well as the use of normalized capacitances versus g_m/I_D are justified.

Finally, semi-empirical and analytical MOST models are introduced, discussing their differences, pros and cons. As in this work we use the former, its election is grounded, especially when nanometer technologies are involved.

2.1.1 MOS transistor inversion regions

The classical and widely used MOS transistor model I-V equation, valid only in strong inversion (and saturation) is

$$I_D = \mu C'_{ox} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}), \qquad V_{DS} \geq V_{GS} - V_T, V_{GS} \geq V_T \tag{2.1}$$

where V_{GS} and V_{DS} are the MOST gate-source and drain-source voltages, V_T is the threshold voltage, μ is the carriers' mobility, C_{ox} is the gate thin oxide capacitance and λ is the Early voltage factor. This equation is considered to be valid for $V_{GS} \geq V_T$. When the gate-bulk voltage is lower than the threshold voltage, there is no significant inversion channel in the transistor and therefore the drain current I_D is zero. In practice, the inversion charge in the channel is gradually reduced as the gate-source voltage decreases, as seen in the plot of Fig. 2.1, where the current I_D versus V_{GS} is plotted in a logarithmic scale. The logarithmic plot shows that below the threshold voltage V_T the current is not zero and has an exponential relation with the gate-source voltage. This current is often referred to as sub-threshold current.

The drain current behavior changes with the gate voltage because the conduction mechanisms change. This idea is briefly explained as follows. In this sub-threshold region the main current conduction mechanism is through diffusion, where the current is proportional to the charge concentration gradient. The diffusion current component, negligible in the above-threshold operation, is also the main mechanism in a bipolar transistor, which shares with the MOS sub-threshold region the characteristic of having an exponential voltage to current function. Above the threshold, the dominating current conduction mechanism is drift, where

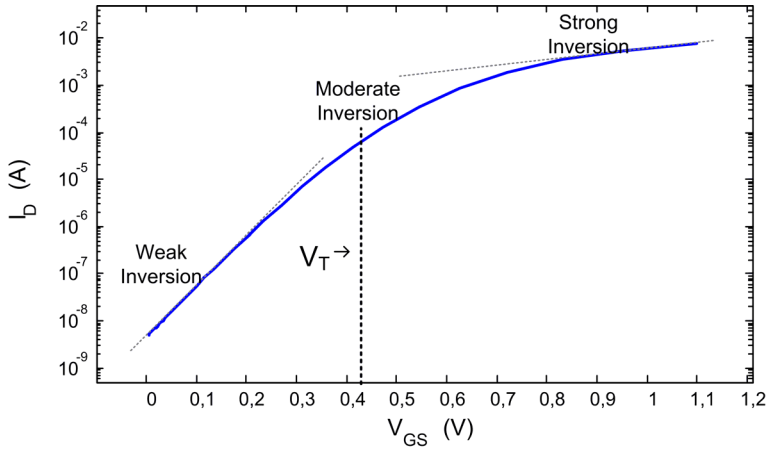


Figure 2.1: *I_D versus V_{GS} for an nMOS transistor with an aspect ratio of $W/L = 6\mu m/100nm$.*

the current is proportional to the inversion charge concentration, leading this mechanism to the classic quadratic relationship between gate voltage and drain current.

Summarizing, depending on the gate voltage value, three behavioral regions of the MOS transistor can be distinguished, as Fig. 2.1 shows:

- *Strong inversion* (SI): when V_{GS} is higher than 100mV of the threshold voltage V_T, the inversion channel is strongly established, the drift current is the dominant. Here it is valid the $I_D - V_G$ MOS equation (2.1).

- *Weak inversion* (WI): for low V_{GS} voltages, far below V_T, the number of free charge is very small, so the inversion in the channel is weak. Here the dominant method of conduction is diffusion and the current I_D has an exponential relationship with V_{GS} ($I_D \propto e^{V_{GS}/(nU_T)}$); that is why $log(I_D)$ in Fig. 2.1 has a constant slope in this zone. Parameter n is the slope factor and U_T is the thermal voltage.

- *Moderate inversion* (MI): when V_{GS} is around V_T both conduction mechanisms are significant and the final effect is a mixture of them. It is easy to see that the mathematical expression in this zone is neither quadratic nor exponential.

When the g_m/I_D feature is presented we will redefine the limits between these regions for more convenient ones, which will be used in the rest of this dissertation.

2.1.2 Analytical and semi-empirical MOST models

As it has been presented in Chapter 1 there are three type of device models. For the MOST models we can characterize them into the following three categories: (1) analytical equation physically-based models, (2) empirical models obtained from measurements, which can be analytical models based on curve fitting or merely look-up tables, and (3) semi-empirical models either analytical models which parameters are described by LUTs, or LUTs obtained from physical models by means of electrical simulation.

In the first category it is included the MOS transistor in saturation classical model given by the well-known and very-simplified drain current-gate voltage quadratic equation presented in (2.1), only useful for strong inversion. In that category there are also included the physical equation-based models valid for all-inversion regions, as PSP [Gild 06], ACM [Cunh 98], EKV [Enz 06], BSIM [He 03, BSIM 08] or HiSIM [Miur 96], used to analytically design in all the regions of operation, especially in moderate and weak inversion regions. These first-category models have proved to be very useful in micro and submicrometer

technologies, because the second-order effects are not very noticeable, so the number of parameters in the equations are extremely reduced. Nevertheless, for CMOS nanometer technologies, MOS transistor second-order (and even third-order) effects have become more and more noticeable with the channel length reduction. To describe these effects, the analytical models incorporate new parameters, not considered before, resulting in more complex models, as shown in [Enz 06, Galu 07]. This complexity and the time needed to adjust these parameters is one of the reasons why semi-empirical models are a convenient choice and are used in this work. To justify these considerations, we provide an example of an analytical model, initially discarding second-order effects -hence having a basic model- and afterwards adding them.

- **An analytical model: ACM**

ACM is an MOST analytical equation physically-based model which covers all-inversion regions of operation. When the MOST behaves without any second-order effects (i.e. for micrometer technologies), the ACM equations are quite simple, with few parameters to adjust. But, when the transistor has short and narrow channel effects, these basic set of equations should be modified to incorporate them, complicating considerably the basic model as it is shown afterwards. In this brief section, a basic set of equations of the ACM model, taken from [Galu 99], is listed down as well as the modifications needed to cope with higher-order effects. It will help to see the model's benefits but also its difficulties when using it for nanometer technologies.

The ACM model defines the specific current I_S,

$$I_S = \frac{W}{L}\frac{U_T^2}{2}\mu n C'_{ox} \tag{2.2}$$

being W and L the MOST width and length, respectively, C'_{ox} the normalized MOST oxide capacitance, U_T the thermal voltage, n the slope factor [Tsiv 00] and μ the effective mobility.

The drain current I_D is expressed as the difference of a forward $I_F = f_F(V_G, V_S)$ and a reverse $I_R = f_R(V_G, V_D)$ currents (with V_D, V_S and V_G -drain, source and gate voltages- referred to the bulk voltage) as follows

$$I_D = I_F - I_R. \tag{2.3}$$

Considering that in saturation region I_D depends slightly with V_D, $I_R << I_F$ and then last equation can be approximated as

$$I_D \cong I_F. \tag{2.4}$$

If the pinch-off voltage is $V_P = (V_G - V_{T0})/n$ [1], the expression that relates V_G with the normalized current i_f is:

$$V_P - V_S = U_T\left(\sqrt{1-i_f} - \sqrt{1-i_P} + ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_P}-1}\right)\right) \tag{2.5}$$

where $i_f = I_F/I_S$ and i_P is i_f at pinch-off, generally around 3. In saturation, the source transconductance g_{ms} is,

$$g_{ms} = \frac{\partial I_D}{\partial V_S} = 2\frac{I_S}{U_T}(\sqrt{1+i_f}-1) \tag{2.6}$$

and the gate transconductance, or simply the MOS transconductance, is

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{g_{ms}}{n}. \tag{2.7}$$

The g_m/I_D ratio can be written as a function of i_f as

$$g_m/I_D = \frac{2}{nU_T}\frac{1}{\sqrt{1+i_f}+1}. \tag{2.8}$$

As an example of a capacitance expression, the C_{gs} is

$$C_{gs} = 2/3C_{ox}\left(\sqrt{1+i_f}-1\right)\frac{\sqrt{1+i_f}+2}{\left(\sqrt{1+i_f}+1\right)^2} \tag{2.9}$$

Other small-signal parameters as drain transconductance g_{md} and bulk transconductance g_{mb}, intrinsic capacitances [Galu 99], linearity [Arna 03], noise [Arna 04] or mismatch [Galu 05] are also written in terms of i_f.

All previous equations depend on the factor n, the mobility factor μ and V_{T0}. If we consider second order effects due to short-channel MOST, these parameters vary respect to long-channel values. The next three effects exemplifies these changes:

1. *Drain-Induced Barrier Lowering (DIBL)*: This effect is clearly visible in short channel MOST, due to the appearance of deeper depletion region and larger surface potential, which reduce the effective threshold voltage and hence, the barrier that V_{GS} has to overcome. Namely, it increases the expected channel current predicted with long-channel theory. If V_{DS} increases for a fixed V_D, the depletion region around drain widens, decreasing even

[1] With V_{T0} defined as $V_{T0} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}$, being V_{FB} the flat-band voltage, ϕ_F the Fermi potential and γ_B the body effect coefficient.

more the effective threshold voltage. It makes the pinch-off voltage to depend on V_G, V_S and V_D, instead of only V_G (see [Tsiv 00], Section 6.3 and [Galu 07], Section 4.7.4)

$$V_P(V_G, V_S, V_D) = V_{P0}(V_G) + \frac{\sigma}{n}(V_D + V_S) \tag{2.10}$$

where σ is the DIBL factor and it is roughly proportional to $1/L^2$ and V_{P0}, the pinch-off voltage when V_D=V_S, is

$$V_{P0} = \left(\sqrt{V_G - V_{T0} + 2\phi_F + \gamma_B\sqrt{2\phi_F} + (0.5\gamma_B^{'})^2 + U_T} - 0.5\gamma_B^{'}\right)^2 - \phi_{S0} \tag{2.11}$$

with V_{T0} the threshold voltage at equilibrium, ϕ_F the Fermi potential, γ_B is the body effect coefficient, ϕ_{S0} is approximately twice ϕ_F and

$$\gamma_B^{'} = \gamma_B - \frac{\varepsilon_0\varepsilon_{Si}}{C_{ox}^{'}}\left(2\frac{\eta_L}{L} - 3\frac{\eta_W}{W}\right)\sqrt{\phi_{S0}} \tag{2.12}$$

where γ_B is the body effect coefficient of a wide and long MOST and $\gamma_B^{'}$ includes the short and narrow effects on the constants η_L and η_W; ε_0 is the vacuum permitivity and ε_{Si} is the silicon relative permitivity. It is clear that to adjust the new expression the parameters η_L, η_W, and σ should be obtained by fitting.

2. *Mobility degradation*: The mobility changes from the zero-bias mobility μ_0 to an expression dependent on the body effect coefficient γ_B and a fitting parameter, generally denoted θ:

$$\mu_{bodyeffect} = f_\mu(\mu_0, \theta, \gamma_B). \tag{2.13}$$

3. *Velocity saturation*: In short-channel MOST, the hypothesis of a carrier velocity proportional to the value of the longitudinal field at all points of the inversion channel is not longer valid as high longitudinal fields F_y appear in the channel; making the velocity saturation effects more evident. The mobility is reduced due to the velocity limit of the carriers, v_{sat} (see [Tsiv 00], Section 6.5 and [Galu 07], Section 4.2), and its expression is

$$\mu_{ve_{sat}}(y) = \frac{\mu}{1 + |F_y|/F_C} \tag{2.14}$$

with the low field mobility $\mu = v_{sat}/F_C$, with F_C the critical longitudinal field and F_y the longitudinal field. F_C is a fitting parameter in the short-channel model when this effect occurs.

• **Semi-empirical models**

The effects included in the previous section show the need to adjust a growing set of constants with fitting parameters for an analytical model in order to correctly use its set of equations for nanometer technologies.

This methodology can be simplified by using the semi-empirical model of Jespers [Jesp 10], where instead of using the complex model with all the set of parameters, the basic model with only three parameters (n, μ and V_{T0}) is considered. These parameters are in LUTs linked to the equations by the parameter i_f or V_G.

In this dissertation, we apply the semi-empirical model approach defined in Chapter 1, extracting by electrical simulation a small set of LUTs of specific low-frequency MOST characteristics. This approach considers jointly second and higher order effects of nanometer technologies.The data are easily obtained by extracting MOST characteristics via low-frequency simulations. In this thesis the MOST dataset is extracted by using a very specific group of voltages, geometries and minimum MOST length.

The typical corner data of the MOST characteristics are only considered in the methodology flow. However we study these characteristics in slow and fast corners in order to know beforehand their variability, helping us to rely on the design results provided by the technology or to be warned of the possible spread of the circuit features data.

2.2 MOST semi-empirical model description

The MOS transistor semi-empirical model used in this thesis comprises LUTs of the following data:

1. g_m/I_D as function of the normalized current $i = I_D/(W/L)$.

   The dependency of g_m/I_D with W, V_{DS} is slight and in a first approximation it can be neglected if narrow devices are not used.

2. g_{ds}/I_D as function of g_m/I_D and V_{DS}.

   The variation with W is very slight and it is not considered here.

3. Normalized capacitances C'_{ij}, with ij={gs, gd, gb, bs, bd} versus g_m/I_D.

   The spread with W and V_{DS} is reasonably small and it is not included in a first approximation.

4. Thermal noise parameters as function of g_m/I_D, and V_{DS}.

   The variation of noise parameters with W can be neglected in the first approximation.

5. Flicker noise parameter K_F versus g_m/I_D, at the RF working frequency.

   The dependency of K_F with W and V_{DS} is very low and hence not considered here.

6. Overdrive voltage V_{OD} versus g_m/I_D.

   The spread of V_{OD} with W and V_{DS} is very low and it is not included in the LUTs.

The flicker noise parameter K_F depends strongly on the working frequency, but this variation is not included in the LUTs because the methodology proposed here is for a fixed working frequency; hence only the simulated data at that frequency is collected.

For those characteristics mentioned above which depends on W, the approach used in this work has been to consider a small set of values covering the whole width range, which is proved to works correctly for the proposed methodology.

The variations with corners of the referred characteristics are provided in order to deeply describe them, but as it has been already said, they are not used in the design methodology flow. This information only aims to provide more information to the designer.

Next, previous statements are justified, and the typical characteristics of the MOST are shown.

The bulk effect should be considered or not, depending on the circuit designed. A brief discussion of this effect is provided in Section 2.2.7. The MOST characteristics of previous sections are obtained for $V_S = V_B = 0V$.

2.2.1 g_m/I_D characteristic

As mentioned in Chapter 1, the g_m/I_D ratio is a MOST characteristic directly related with the inversion region of the transistor. Next we discuss why this happens.

The coefficient g_m/I_D is the slope of the curve I_D versus V_G in a logarithmic scale because [Silv 96, Fior 12]

$$g_m/I_D = \frac{\partial I_D/\partial V_G}{I_D} = \frac{\partial log(I_D)}{\partial V_G} \tag{2.15}$$

As Fig. 2.1 shows, the maximum slope of the curve, that is, the maximum g_m/I_D ratio, appears in the weak inversion region. Then, it decreases until reaching the strong inversion region. Firstly, it means that weak and moderate inversion regions are more adequate for low power and efficient designs. In these regions, the values of gate voltage V_G (around 100 mV below the threshold voltage) and the overdrive voltage $V_{OD} = V_{GS} - V_T$ are very low, which make these zones very adequate for low supply voltage operation.

The g_m/I_D ratio is a measure of the efficiency to translate I_D into the transconductance g_m, because the greater g_m/I_D value the greater transconductance which can be obtained at a constant current value. Fig 2.2 shows the g_m/I_D curve as a function of I_D (which is the variable used for MOS biasing) for an nMOS transistor. The maximum value of g_m/I_D is approximately $1/nU_T$; for TECH1 this value is approximately 28 V^{-1}.

Lets study the limits of SI, MI and WI, considering g_m/I_D. For micrometer technologies the definition of these limits came from (2.8): WI was defined for $i_f << 1$ as $g_m/I_D \cong 1/nU_T$, and SI was defined for $i_f >> 100$. Now, for nanometer

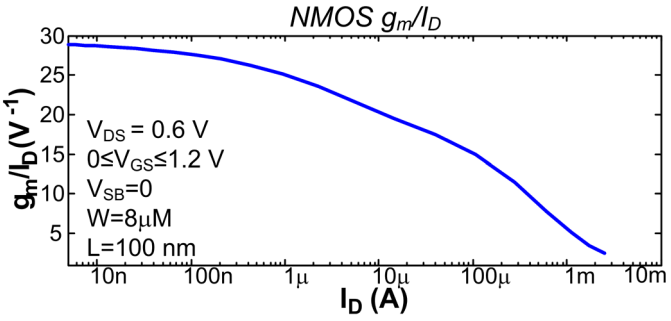


Figure 2.2: *g_m/I_D vs. I_D for an nMOS transistor with an aspect ratio of W/L=8µm/100nm.*

technologies, where I_S changes with the transistor biasing, and where (2.8) is not longer valid without considering second order effects, the referred limits cannot be considered so strictly, and the limits are somewhat blurred. For TECH1, we consider these tentative limits as follows: for g_m/I_D higher than 20 V^{-1} this transistor is in weak inversion, for g_m/I_D lower than 10 V^{-1}, it is in strong inversion, and for g_m/I_D in the midst of this range, it is in moderate inversion.

- g_m/I_D **versus transistor size**

To maintain the g_m/I_D ratio while increasing the transconductance g_m, the transistor size should be modified, as it is discussed in this section.

MOST drain current is expressed as function of the gate, source and drain voltages and of the aspect ratio W/L, as follows

$$I_D = \frac{W}{L} f_1(V_G, V_D, V_S; L, W). \tag{2.16}$$

Function f_1 is usually named normalized current $i = I_D/(W/L)$; its dependences with transistor length L and width W are explicitly considered only for short or narrow channel MOS, respectively, as the variations are very slight. Then, applying the definition of transconductance g_m together with the expression (2.16), it is obtained

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} \frac{\partial f_1(V_G, V_D, V_S; L, W)}{\partial V_G}. \tag{2.17}$$

Finally, from expressions (2.16) and (2.17), the g_m/I_D ratio is written as

$$g_m/I_D = \frac{\partial f_1/\partial V_G}{f_1} = \frac{\partial (log f_1)}{\partial V_G} = \frac{\partial \Big(log\big(I_D/(W/L)\big) \Big)}{\partial V_G} = f_2(I_D/(W/L)) = f_2(i). \tag{2.18}$$

Because ideally $i = f_1$ does not depend on the transistor width W for MOS transistors with equal length, the g_m/I_D ratio is determined by i. In the real world, i has a slight dependence with W and L -because of the I_D dependence expressed in (2.16)- Therefore, for different transistor widths or lengths, variations of g_m/I_D versus i with W or L are very slight.

Considering a fixed transistor length, expressions (2.17) and (2.18) indicate that to increase g_m while maintaining a high value of g_m/I_D, W should be increased maintaining constant $I_D/(W/L)$ (and consequently g_m/I_D), while increasing I_D. As a drawback, increasing W means increasing the parasitic capacitances, which implies reducing the transistor f_T. These two opposite factors (maintaining or improving g_m/I_D when increasing both W and I_D but increasing the parasitic capacitances) show the existence of an optimum in the compromise bandwidth-consumption ($f_T \leftrightarrow I_D$) which generally appears in the moderate inversion region.

Table 2.1: *nMOS characteristics for SI, MI and WI*

g_m=5mS	SI	MI	WI
g_m/I_D (V^{-1})	4	14	25
I_D (mA)	1.25	0.36	0.20
i (μA)	17.8	0.79	0.012
W (μm)	7	45	1590
$C_{gs}+C_{gd}+C_{gb}$ (fF)	5	27	400
$f_T/10$ (GHz)	16	3	0.2
V_G (V)	0.85	0.56	0.36

To comprehend quantitatively this idea, these dependences are shown in Table 2.1 where, for a given transconductance g_m =5 mS, the impact of operating in strong, moderate or deep weak inversion is shown. In weak inversion, current is reduced but the transistor area increases dramatically, whereas one tenth of f_T crumbles below the gigahertz. In strong inversion, the drain current is more than six times higher than in weak inversion, but the transistor width is more than two hundred times smaller than in weak inversion and the quasistatic-limit frequency is higher than fifteen gigahertz. With moderate inversion an equilibrium in obtained, as the transistor width is not so high, the power consumption falls 3.5 times respect to strong inversion and the quasistatic-limit frequency is in the middle. In conclusion, working in moderate inversion region allows decreasing consumption while keeping acceptable frequency and die area characteristics.

From the above discussion, we can state that the curve g_m/I_D versus i can be considered a technological characteristic which value for a particular i varies a little when the transistor width changes. This potential is fully exploited throughout this dissertation, and it will be our fundamental design tool. This relation is strongly related to the performance of analog circuits and gives an indication of the transistor region of operation. Also, the g_m/I_D versus i curve provides a tool for calculating transistor dimensions, as it has been discussed in Section 1.1. As

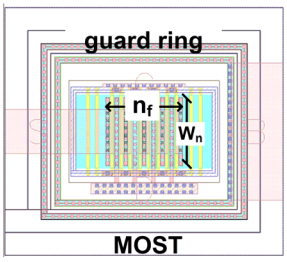


Figure 2.3: *Layout of MOST for TECH1, showing its physical parameters, W_n and n_f.*

already mentioned, this curve slightly varies with the transistor width and length, and only changes appreciably for narrow or very short channels. For TECH1 and TECH2, this curve is extracted for the minimum transistor length (100 nm) and a set of four widths W={1, 10, 100, 320} μm. This small range is enough for covering very well the variations of g_m/I_D vs. i in the whole transistor region. Because of the slight variation in the curve g_m/I_D vs i with the transistor dimensions, the methodology presented here makes sense.

For TECH1, the behavior of g_m/I_D vs. i for nMOS and pMOS transistors -which typical layout shown in Fig. 2.3- , for minimum channel length, is visualized in Fig. 2.4.(a) and (b) with the MOST width varying between W=2 μm and W=320 μm, sweeping MOST finger width, W_n, and MOST number of fingers, n_f.

For this technology there is an appreciable difference between nMOS transistor with W_n=1 μm and higher width fingers due to narrow channel effects, especially in moderate and weak inversion, as shown in the green curve of Fig. 2.4.(a). For higher finger widths, the differences in the curve of the g_m/I_D ratio are not distinguishable. So, the assumption than the g_m/I_D ratio for a given i is almost constant, is valid if narrow devices, which are not usually applied for transconductance generation in radiofrequency, especially in moderate and weak inversion, are not considered.

The overdrive voltage V_{OD} is classically used in radiofrequency designs, as in the works of Shaeffer and Lee [Shae 97] or Belostotski [Belo 06]. The top axis of Fig. 2.4.(a) shows the overdrive voltage values that corresponds to the normalized current i at the bottom axis.

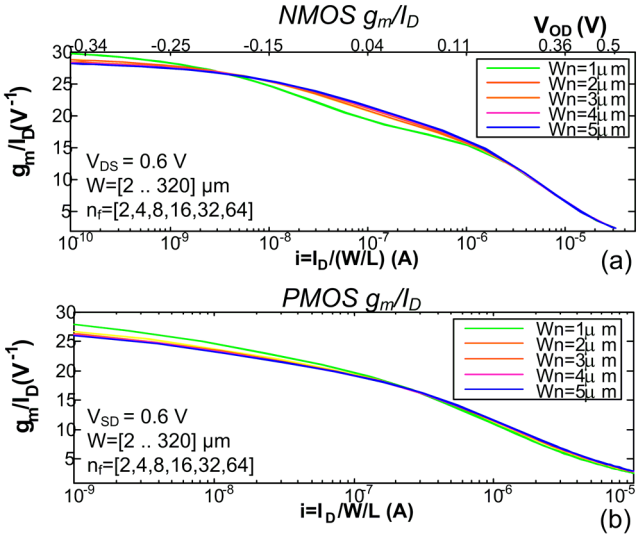


Figure 2.4: *(a) nMOS g_m/I_D vs. i and vs. V_{OD} and (b) pMOS g_m/I_D vs. i.*

- g_m/I_D **with drain-voltage and technology variations**

Lets see now the g_m/I_D ratio spread variations with the V_{DS} voltage, which are presented in Fig. 2.5 for V_{DS}={0.3, 0.6, 0.9, 1.2} V, n_f={1, 4, 16, 64} and W_n={2, 3, 4, 5} μm. It is noticeable a deviation when V_{DS}=0.3 V, but it is not so large to be considered. Previous results show that g_m/I_D versus V_{DS} variations do not modify considerably the g_m/I_D curve, and hence the circuit characteristic in which this transistor is embedded.

Lets see now the g_m/I_D variations with technology parameters. Considering typical, fast and slow corners of the technology TECH1 in Fig. 2.6, we observe a very slight variation in the g_m/I_D ratio. This reinforces the idea of utilizing it as the basis of the methodology we will describe later on.

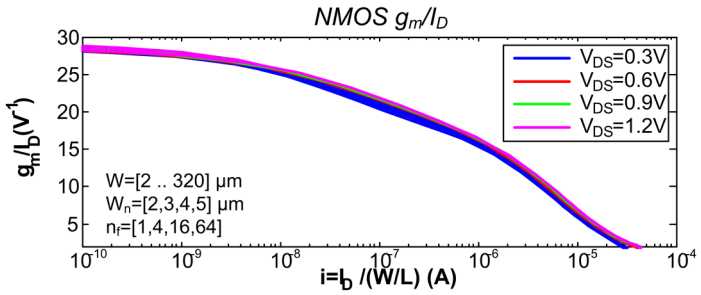


Figure 2.5: *g_m/I_D versus i for four V_{DS} voltages.*

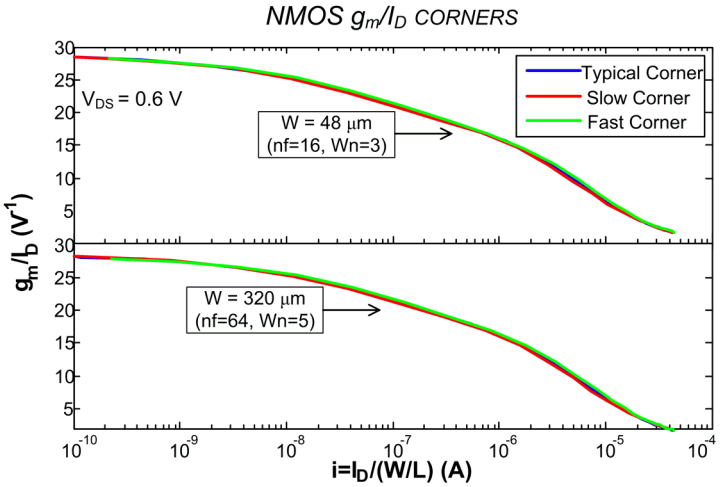


Figure 2.6: *nMOS g_m/I_D corners (typical, fast and slow) versus i.*

- f_T **versus** g_m/I_D

The transition frequency definition is

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd}+C_{gb})} \tag{2.19}$$

where C_{gs}, C_{gd} and C_{gb} are the gate-source, gate-drain and gate-bulk capacitances of the MOST. As g_m and capacitances can be expressed versus g_m/I_D, f_T is a function of g_m/I_D, as it is appreciated for nMOS and pMOS transistors in Fig. 2.7.[2] These curves give us an idea of the frequency limits of nMOS and pMOS transistors of TECH1 using minimun channel length for different inversion regions.

These figures show that for an nMOS transistor biased in SI, f_T can surpass one hundred gigahertz and pMOST reaches fifty gigahertz. In deep WI those frequencies drop down to levels below the gigahertz. For the nMOS transistor of Table 2.1 and considering again the very restrictive quasi-static limit for the working frequency f_0 of one tenth of f_T, for a g_m/I_D around 4 V^{-1}, f_0 can be up to the tens of gigahertz, whereas with a g_m/I_D around 25 V^{-1} f_0 falls below the gigahertz. This simple check lets the designer to know the limitations of the technology in terms

[2]The plots comparing the g_m/I_D and f_T as functions of i is presented in Appendix 2.A, Fig. 2.38.

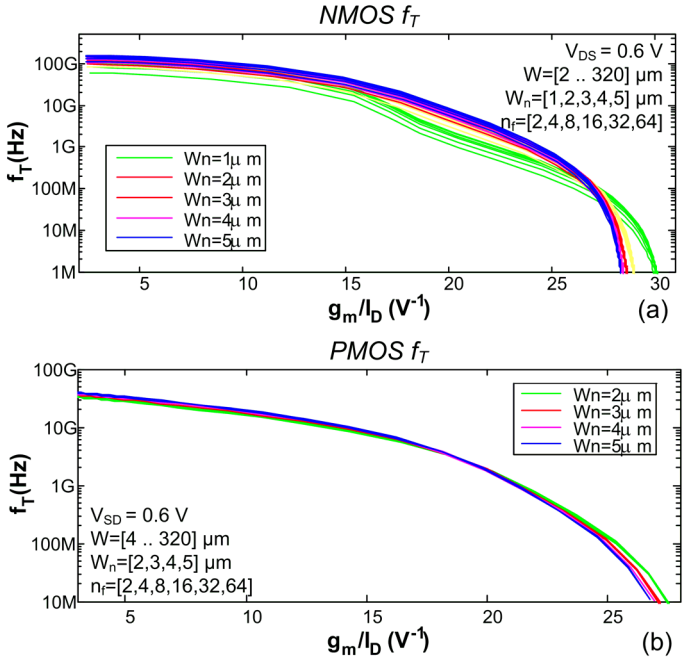


Figure 2.7: *(a) nMOS and (b) pMOS f_T versus g_m/I_D.*

of frequency in each level of inversion. [3]

2.2.2 Output conductance g_{ds} and g_{ds}/I_D ratio

Another fundamental small-signal parameter required in our methodology to describe the MOST behavior is the output conductance g_{ds}. It dramatically increases in nanometer transistors with respect to micrometer ones due to the shortening of the channel length, as it is, in a first approximation, inversely proportional to the transistor length L [Tsiv 00]. This effect should be considered because it could strongly influence certain RF blocks. For example, in an LC tank-VCO the conductance g_{ds} affects the value of the final MOS transconductance chosen, and hence the bias current and the phase noise; in an LNA a high g_{ds} value reduces the maximum gain of the circuit.

The g_{ds}/I_D ratio, similar to the g_m/I_D ratio, is applied here [Jesp 10]. Figure 2.8 shows the behavior of g_{ds}/I_D versus g_m/I_D[4]. The g_{ds}/I_D range is very small, moving from 0 to 2 V^{-1}, and no appreciable change in g_{ds}/I_D is seen when W_n is higher than 1 μm.

The g_{ds}/I_D ratio decreases when moving towards strong inversion, which happens because $g_{ds}/I_D \cong 1/V_A$, where V_A is the Early voltage in first-order channel length modulation formula, and as Tsividis stands, in Sections 6.2 and 8.2 of [Tsiv 00] $V_{AW} < V_{AS}$ with V_{AW} and V_{AS} the Early voltage for weak and strong inversion regions, respectively.

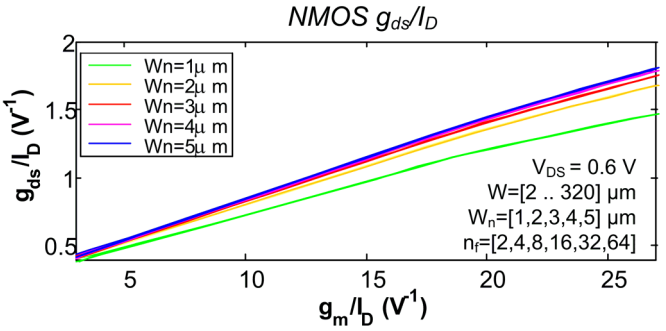


Figure 2.8: *nMOS g_{ds}/I_D versus g_m/I_D.*

[3] A brief comment concerning the election of the unitary transistor width W_n is that, as expected, it is recommendable to use transistors with high W_n (and so, less n_f) in moderate and weak inversion, to reduce the parasitic capacitances. At the limit, for transistors with W_n=1 μm the f_T substantially drops in moderate inversion regions.

[4] The behavior of the g_{ds}/I_D ratio versus i is presented in Fig. 2.39.

- g_{ds}/I_D **with drain voltage and technology variations**

Contrary to what happens with the g_m/I_D ratio, the g_{ds}/I_D ratio appreciably changes with the drain-source voltage V_{DS}, which is expected due to the direct relation of g_{ds} with the drain voltage. In Fig. 2.9, the g_{ds}/I_D ratio is plotted versus g_m/I_D, for four drain voltages, where the variation is clearly appreciable. A decreasing tendency of the g_{ds}/I_D curve is observed when drain voltage increases. In weak and strong inversion regions g_{ds}/I_D changes around 0.7 V^{-1} and 0.4 V^{-1}, respectively.

The corners variations of the g_{ds}/I_D parameter are presented in Fig. 2.10. In order to provide a typical example, only the corners obtained with V_{DS}=0.3 V are plotted. The high spread of g_{ds}/I_D between typical and fast and slow corners reaches 0.5 V^{-1}.

The g_{ds} MOS parameter has a considerable spread with variations in the drain voltage and in the technology characteristics. These facts make us expect some differences between computational data and simulations if the correct drain voltage is not chosen; and between computational data and measurements if the process moves from typical corner.

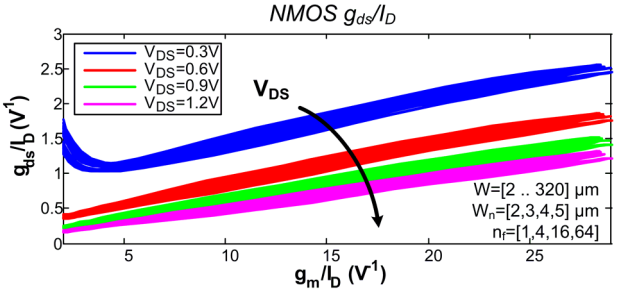


Figure 2.9: *g_{ds}/I_D versus g_m/I_D for four drain voltages.*

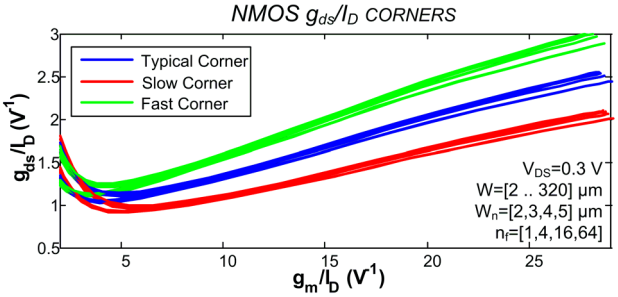


Figure 2.10: *nMOS g_{ds}/I_D corners versus g_m/I_D, for V_{DS}=0.6 V.*

2.2.3 MOST extrinsic and intrinsic capacitances

Working in radiofrequency compulsory requires the inclusion of transistor capacitances in the MOST modeling, which are grouped in intrinsic and extrinsic ones. They influence not only on the f_T computation but also on the input and output impedances of the MOS, the MOST gain and noise, among other characteristics.

In this thesis, the extrinsic capacitances are modeled with the known expressions of [Tsiv 00] (Section 8.4, pages 405-410):

1. the extrinsic gate-source (and gate-drain) capacitances C_{gse}=C_{gde}=$WC_o^{''}$, with $C_o^{''}$ the capacitance per unit width that includes the fringe, the overlap and the top gate contributions.

2. the extrinsic gate-bulk capacitance $C_{gbe} = 2LC_{ob}^{''}$, where $C_{ob}^{''}$ is the capacitance per unit length.

3. the junction substrate-source and substrate-drain capacitances $C_{bse} = C_{bde} = A_{S(D)}C_{js(jd)}^{'} + l_{S(D)}C_{jsf(jdf)}^{''} + WC_{jsc(jdc)}^{''}$, with $A_{S(D)}$ and $C_{js(jd)}^{'}$ are the source (drain) area and the capacitance per unit area, $l_{S(D)}$ and $C_{jsf(jdf)}^{''}$ are the source (drain) outer sidewall length and the capacitance per unit length and W and $C_{jsc(jdc)}^{''}$ are the source (drain) inner sidewall length the capacitance per unit length.

The parameters of the extrinsic capacitances are taken from the technology files and from layout considerations.

Respect to the intrinsic capacitances, the study is a bit more complex. Considering again that the working frequencies are below one tenth of f_T, it is enough to consider the following intrinsic capacitances: C_{gs}, C_{gd}, C_{gb}, C_{bs} and C_{bd}, disregarding the other four capacitances and transcapacitances as well as non-quasistatic effects. These capacitances change with the inversion level, as Tsividis states ([Tsiv 00], page 405); and obviously they change with the transistor size. In this work the intrinsic capacitances are considered to be proportional to the gate area (WL). This can be done because these capacitances are proportional to the oxide capacitance C_{ox} which is itself proportional to WL, as Tsividis presents in [Tsiv 00], Section 8.3, page 391. Considering this basic idea, in the LUTs of the MOST there are the normalized capacitances $C_{ij}^{'}$ versus the g_m/I_D.

In Fig. 2.11 it is shown the behavior of the normalized capacitances $C_{gs}^{'}$, $C_{gd}^{'}$, $C_{gb}^{'}$, $C_{bs}^{'}$ and $C_{bd}^{'}$ versus g_m/I_D for V_{DS}=0.6 V and a wide set of MOST widths. Their maximum absolute spread are: (1) the $C_{gs}^{'}$ variation is around 1 mF/m^2; (2) the $C_{gd}^{'}$ spread is around 0.4 mF/m^2; (3) the $C_{gb}^{'}$ error it is less than 0.02 mF/m^2, being the highest perturbation in the MI-WI zone, as the inset of Fig. 2.11.(c) stands; (4) the $C_{bs}^{'}$ variation is 0.02 mF/m^2 and (5) the $C_{bd}^{'}$ error is lower than 0.002 mF/m^2.

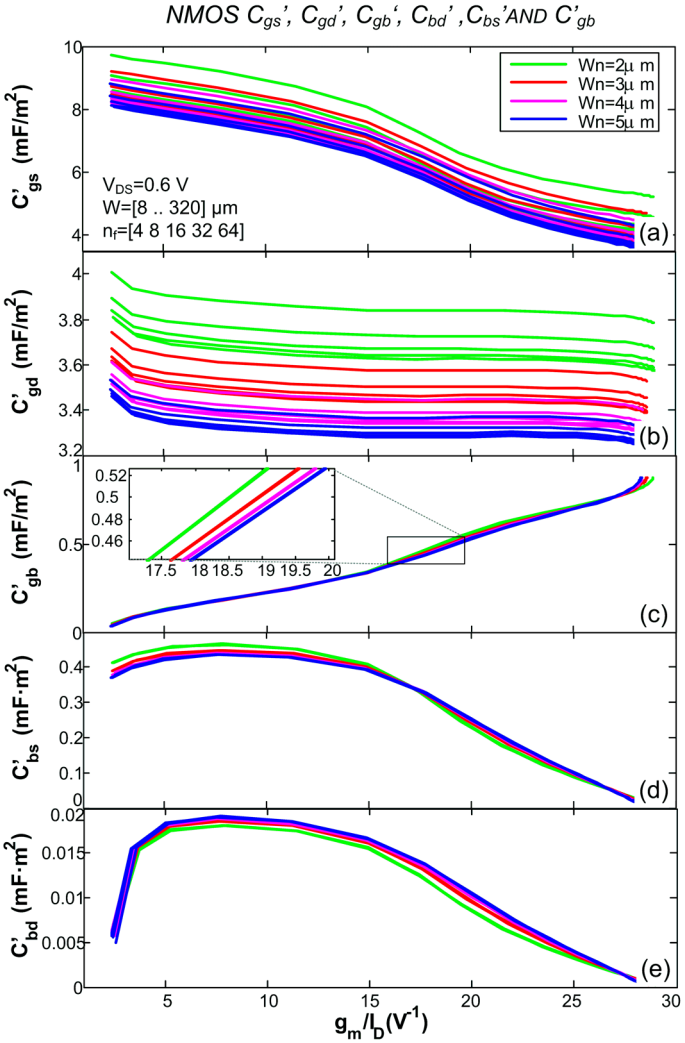


Figure 2.11: *Intrinsic capacitances: (a) $C_{gs}^{'}$, (b) $C_{gd}^{'}$, (c) $C_{gb}^{'}$, (d) $C_{bs}^{'}$ and (e) $C_{bd}^{'}$ versus g_m/I_D. The inset of (c) shows that the highest perturbation of the $C_{gb}^{'}$ is in MI-WI zone.*

Only for $C_{gs}^{'}$ the error is appreciable in weak inversion, where $C_{gs}^{'}$ rounds 4 mF/m^2 and the relative error is around 20%. Despite this error in this region, in the first approach, the normalized capacitance LUTs only consider the variations with g_m/I_D.

Taking into account this basic idea, in the LUTs of the MOST there are the normalized capacitances $C_{ij}^{'}$=$C_{ij}/(WL)$ versus g_m/I_D.

Considering drain-source voltage variations, Fig. 2.12 shows that the spread is very similar that when the width is swept. To study the corners, we extract the $C_{gs}^{'}$ of a MOST with W=8 μm and V_{DS}=0.6 V; which expected slight spread is shown

in Fig. 2.13. In all cases, the tolerances are acceptable for this methodology. Afterwards, normalized capacitances are used to estimate the capacitances of other transistors in the considered width range, only multiplying by the respective WL. With the observed results, a rough capacitance modeling can be obtained by extracting the capacitances of a MOST sized with a middle-range width and biased with a midst-range V_{DS}.

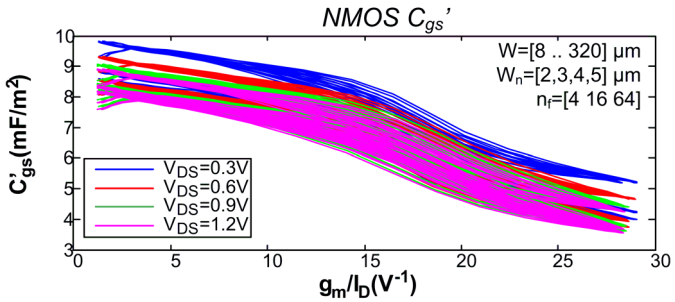


Figure 2.12: C'_{gs} *versus* g_m/I_D *for four* V_{DS}.

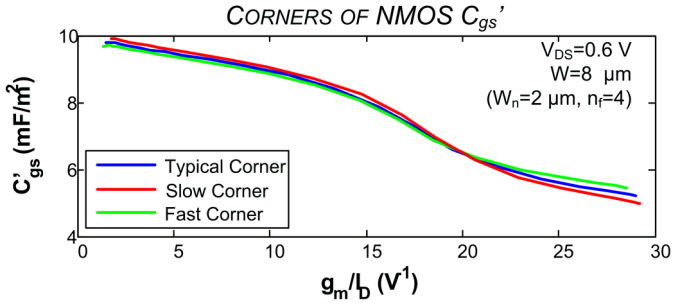


Figure 2.13: C'_{gs} *corners versus* g_m/I_D

2.2.4 Noise in MOS transistors

This section presents the MOS transistor noise sources used throughout this work to deduce the equations that describe the noise characteristics of the radio-frequency blocks. These sources are fundamentally the drain-noise current (consisting of the white noise and the flicker noise) and the induced gate noise, presented in Tsividis ([Tsiv 00] Section 8.5); and more recently, for RF models, by Shi et al. [Shi 09]. The scheme of these noise currents referred at the output drain of the MOS as $\overline{i_o^2}(f)$, as well as its principal contributors are shown in Fig. 2.14.

The output current power spectral density zone is sketched in Fig. 2.14, in which three regions are recognized: the flicker noise zone, the white noise zone and the induced-gate noise zone. The white noise is due to random fluctuations of the charge in the channel, the flicker noise is the result of trapping and detrapping of the channel carriers in the gate oxide. The frequency of the asymptotic limit between these two zones f_c, is called the corner frequency.

The white noise power spectral density (psd) $\overline{i_{w,d}^2}$, for all inversion regions, is expressed as [Galu 99]

$$\overline{i_{w,d}^2} = 4k_BT\gamma g_{d0} = 4k_BT\frac{\gamma}{\alpha}g_m \tag{2.20}$$

where k_B is the Boltzmann constant, T is the absolute temperature, γ is the excess noise factor, α is equal to $\alpha = g_m/g_{d0}$, with g_{d0} the output conductance g_{ds} at $V_{DS} = 0$. g_{d0} is considered because at zero V_{DS} the white noise is maximum for all-inversion regions [Tsiv 00].

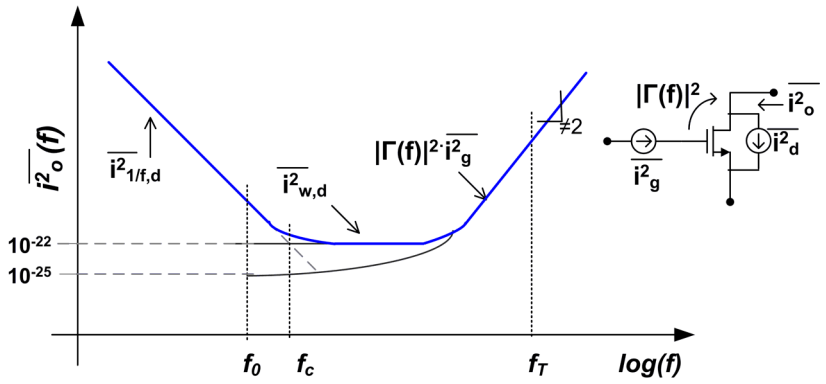


Figure 2.14: *Sketch of the MOST power-spectral density versus frequency; with the gate noise psd and drain noise psd order of magnitudes at f_0 and $|\Gamma(f)|^2$ the transfer funcion of the induced gate noise to the MOST i_o^2.*

The flicker noise psd $\overline{i^2_{1/f,d}}$ is written as

$$\overline{i^2_{1/f,d}} = \frac{K_F g_m^2}{C'_{ox} W L} \frac{1}{f} \tag{2.21}$$

with K_F the flicker noise constant, C'_{ox} the normalized MOST thin oxide capacitance and f is the frequency of study.

The psd of the drain-noise current is $\overline{i^2_d} = \overline{i^2_{w,d}} + \overline{i^2_{1/f,d}}$ as no correlation is supposed to exist between the white noise and the flicker noise sources.

For high frequency operation, the induced gate noise should be considered, as it is pointed out in Fig. 2.14. This noise appears because random fluctuations of the carriers (generated by the white noise) cause a gate current to flow through the gate, even if no signal current exists. Its psd, $\overline{i^2_g}$, is expressed as

$$\overline{i^2_g} = 4k_B T \delta \frac{C^2_{gs}}{5 g_{d0}} 4\pi^2 f^2 = \frac{16}{5} \pi^2 k_B T \alpha \delta \frac{C^2_{gs}}{g_m} f^2 \tag{2.22}$$

where δ is the gate noise coefficient.

The gate noise is partially correlated with the drain noise due to the white noise, with a correlation coefficient c given by Van der Ziel [Ziel 86] and Lee [Lee 04]

$$c = \frac{\overline{i_g i^*_{w,d}}}{\sqrt{i^2_g i^2_{w,d}}} \tag{2.23}$$

with |c| approximately equal to 0.4.

- **Noise constants versus** g_m/I_D

The generally used values of γ, δ and α are $\gamma = 2/3$, δ is two times γ and $\alpha \cong 0.6$. But when working with short channel devices and in moderate and weak inversion, these parameters would take different values. These parameters depend, as happens with other transistor characteristics, on g_m/I_D. So, in order to improve the methodology results, we express these constants in terms of g_m/I_D to include them in the design methodology.

When a fluctuation of these parameters does not modify considerably the noise characteristics of a circuit, it is acceptable to consider them as constants. In Chapter 3 it is provided a set of VCO designs in the mentioned situation. However, when a small change in them modifies the circuit noise characteristics, a deeper study must be done as it happens with the LNAs of Chapter 4.

To show graphically the effects of the inversion region in the noise parameters α and γ, they have been extracted from simulations using a 48 μm$\times$100 nm MOS transistor (with W_f=3 μm and n_f=16) and plotted in Fig. 2.15, for four V_{DS} voltages.

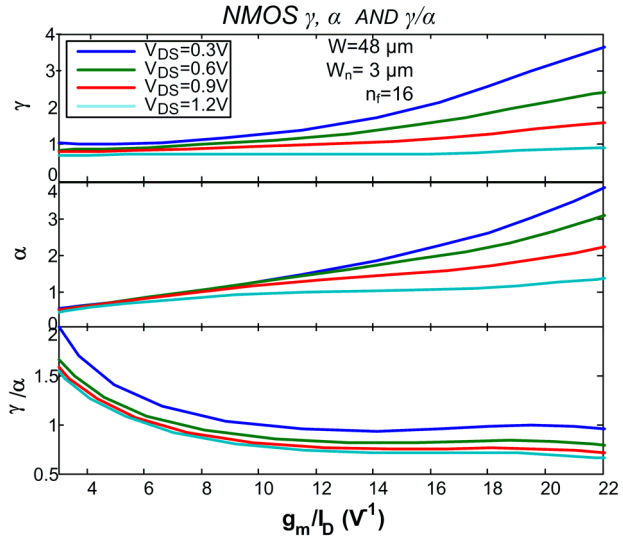


Figure 2.15: *nMOS transistor noise parameters:* γ, α *and* γ/α.

As the relation γ/α also appears in the noise equations of this dissertation, it is also represented there. For strong inversion, γ and α are low, but not always near the generally used values. However, when moving to weak inversion, both variables suffer a dramatical raise. This increment generates circuit noise computation errors if the MOS transistor is in MI and WI and the proper parameter values are not considered. Nonetheless, when considering the γ/α ratio, it is maintained relatively constant.

Extending this study to the process variations, Fig. 2.16 depicts the simulated α versus g_m/I_D considering the four corners, for a set of V_{DS} voltages; as happens with other MOST characteristics, the slight spread observed might not be included in the MOST LUTs.

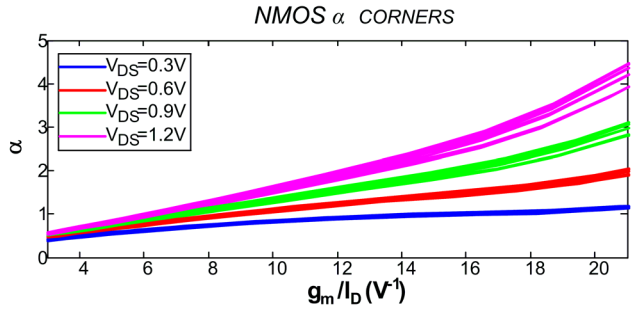


Figure 2.16: α *corners versus* g_m/I_D *for four* V_{DS}.

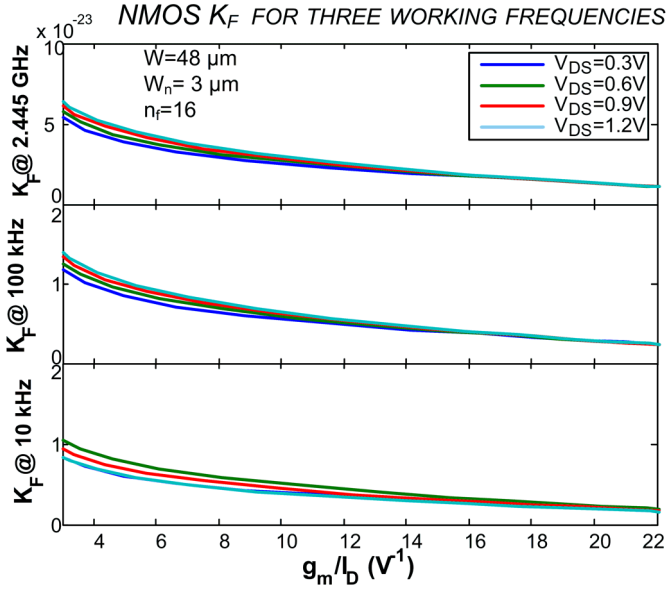


Figure 2.17: *K_F versus g_m/I_D for three frequencies and four V_{DS}.*

Lets now consider the K_F parameter. K_F is solved extracting by simulation the flicker current density and the transconductance while sweeping g_m/I_D. The study is done with a $48\mu m/100nm$ MOST, for three frequencies f_0={2.4 GHz, 100 kHz and 10kHz} and four V_{DS}, as it is presented in Fig. 2.17. No appreciable differences are visualized when varying the drain voltage. However, there is a clear variation of K_F when the working frequency is considered. Table 2.2 lists a set of values of K_F in weak, moderate and strong inversion, for the three frequencies simulated. Two observations arise from observing the presented data: (1) K_F decreases when

Table 2.2: *Comparison of K_F values for SI, MI and WI.*

f_0 (Hz)	g_m/I_D (V^{-1})	K_F ($\times 10^{-24}$) at V_{DS}=0.6 V
2.4 G	5	48
100 k	5	11
10 k	5	8.1
2.4 G	14	22
100 k	14	4.8
10 k	14	3.0
2.4 G	21	12
100 k	21	2.7
10 k	21	1.7

moving to weak inversion for all the frequencies considered, and (2) the estimation of K_F increases for high frequencies.

Concerning the variation with the inversion region, two approaches could be taken. A simple approach is to consider the mean value of K_F through the range of g_m/I_D and an advanced approach is to use look-up tables. Depending on the circuit, the level of accuracy needed in the estimation of the flicker noise and the ratio between $\overline{i^2_{d,1/f}}$ and $\overline{i^2_{d,w}}$ is the approach that should be considered. For example, in the LNA design methodology of Chapter 4 it is used the simple approach.

Noise parameters vary very slightly with the transistor width (with a relative error of less than a 5% for γ/α and K_F), so this variation is not considered here.

Further reading on these topics can be found in the studies presented by Manghisoni et al. [Mang 06], Scholten et al. [Scho 04] or Chan et al. [Chan 06]. These works quantify the constants of the power spectral densities of MOS transistor noise sources particularly for nanometer technologies.

2.2.5 Overdrive voltage versus g_m/I_D

As it is expressed in (2.5), the overdrive voltage is function of the normalized current, and hence of the g_m/I_D ratio. It means that the designer has a way of directly estimate the value of V_{GS} when the g_m/I_D ratio is fixed. As happens with other MOS transistor characteristics, it varies slightly with the MOST width, as it is shown in Fig. 2.18.

It has been studied the variation of the overdrive voltage with the drain-source voltage, presented in Fig. 2.19 and its spread with the corners (typical, fast and slow), for a fixed drain-source voltage, plotted in Fig. 2.20. As well as happens with the MOST width variations, the maximum spread considering the V_{DS} variations is around 0.03 V, then it is not needed to include these variations in the LUTs. The variations with the corners are around the same value.

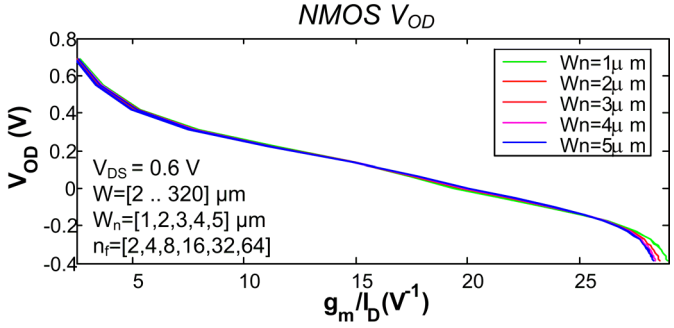


Figure 2.18: *Overdrive voltage versus g_m/I_D varying the transistor width, for V_T=0.41 V*

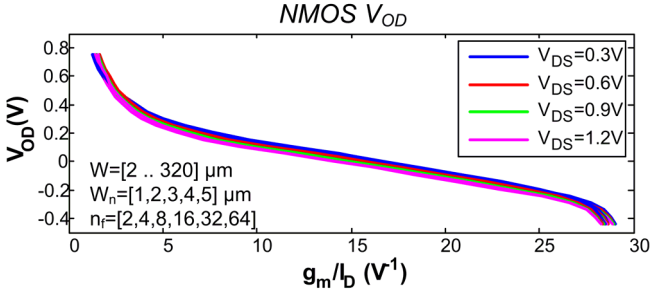


Figure 2.19: *Variations with the V_{DS} of the overdrive voltage versus g_m/I_D .*

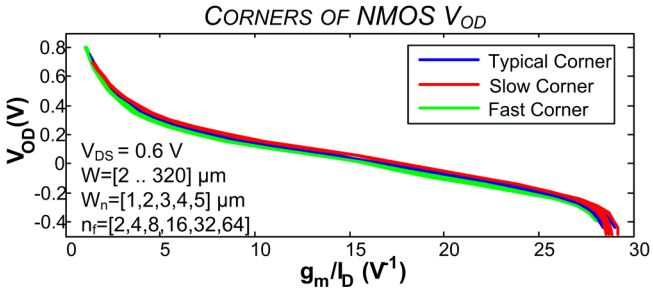


Figure 2.20: *Corners of the overdrive voltage versus g_m/I_D varying the transistor width.*

2.2.6 Bulk substrate effect

This is considered a second order effect because g_{mb} is much smaller than g_m, as it is shown in Fig. 2.21. However it should be included in the LUT, especially if this effect is important in the circuit behavior. For other circuits, where the bulk is short-circuited with the source terminal, it is discarded.

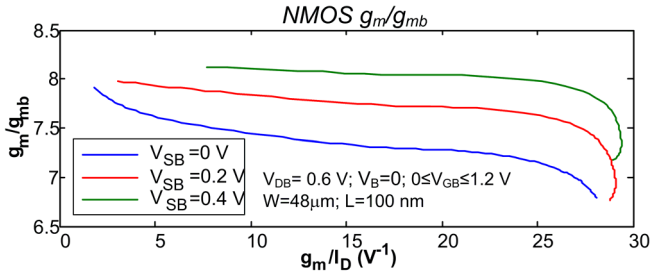


Figure 2.21: *g_m/g_{mb} ratio as function of g_m/I_D.*

For the common-source LNA of Chapter 4, the bulk effect present in the cascode MOST is neglected because this transistor affects in a much less extend the LNA behavior respect to the MOST amplifier. For the VCO, only the pMOS transistors have the bulk effect, but in the first approach is has been discarded to simplify the set of equations presented.

2.2.7 MOS transistor data acquisition scheme

To conclude, for the proposed methodology five MOS transistor basic characteristics must be considered, for a fixed V_{DS}:

1. the transconductance to current ratio g_m/I_D,
2. the output conductance to current ratio g_{ds}/I_D,
3. the normalized MOS capacitances $C_{ij}^{'}$=$C_{ij}/(WL)$,
4. the noise constants
5. the overdrive voltage

To acquire these LUTs, the simple scheme of Fig. 2.22 is utilized. In it, MOS transistor gate, drain and source nodes are connected to a DC voltage source, while source and bulk nodes are connected either to ground (nMOS transistor) or to the supply voltage (pMOS transistor). V_G is swept extracting I_D, g_m, g_{ds} and $C_{ij}^{'}$. V_D and V_S are set around their expected DC value. The same simulation must be run for a set of widths -for example, the mentioned set of {1, 10, 100, 320} μm-,for a fixed transistor length. If the transistor length also changes, following the same idea, a small set of lengths (e.g. 100 nm, 1 μm, 10 μm) should be chosen. For the noise parameter extraction, an AC noise analysis has to be done.

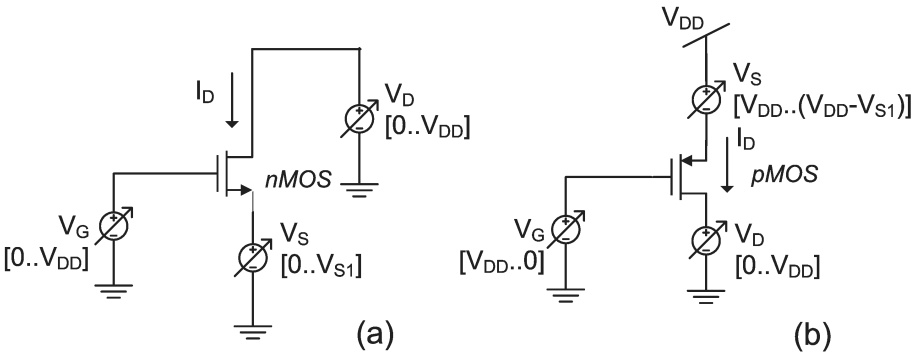


Figure 2.22: *Test circuit for acquiring MOST g_m/I_D, g_{ds}/I_D and $C_{ij}^{'}$.*

2.3 Passive component semi-empirical models

In radiofrequency design, on-chip passive components need to be correctly characterized, since the performance of the circuit strongly depends on them. For example, in a VCO design, if the model of the tank inductor considers a parasitic parallel resistor much lower that the real one, the VCO could even not oscillate. This section briefly introduces the models and parameters of the passive components we will use in the designs of Chapters 3 and 4.

The passive components can be modeled either with analytical models or with semi-empirical ones. The former are especially useful in multi-frequency systems. However obtaining simple and accurate formulae for the element and its parasitics is somewhat difficult. In this thesis we decided to use semi-empirical models extracted from electrical simulations, the same way we do with the MOS transistor modeling. Depending on the level of accuracy and the available technological information, the models can be extracted using the parametrized cells provided by the foundry libraries or the ones obtained with electromagnetic simulators as ADS Momentum, ASITIC [Nikn 00] or VPCD of Cadence [VPCD 09]. Two main drawbacks of electromagnetic simulators exist: 1) the need to have the technological data provided by the foundry to obtain accurate descriptions, and 2) the high computational time spent to obtain the solutions. In this thesis, in order to speed-up the design, the former method is utilized; the library cells supplied by the foundry are simulated using AC analysis at the working frequency obtaining their equivalent complex impedance.

This thesis uses simple AC passive component models, as an ideal inductor in series with a parasitic resistor for on-chip inductors. Biunivocal relations between the model parameters of the component are very useful to generate a simple design flow, as for example between the inductor inductance and its parasitic serial resistance The extraction of these models depends on the topological location of the component; for example, if the device has an AC grounded terminal or it is fully differential. The analysis performed with the electrical simulator has to reflect this fact.

In the following study, a simple modeling of the inductors, capacitors, varactors and resistors is presented as well as their principal characteristics and their parasitics. Despite the varactors are, in fact, based on active devices, we include their study in this section. We do this because we characterize the varactor, for each value of its control voltage, as a capacitor with its equivalent capacitance and its parasitic resistance.

2.3.1 Inductor modeling

In this thesis we use the inductors cells provided by the foundry. The extracted inductor model consists on an equivalent ideal inductor with a parasitic resistor for the working frequency f_0. Depending on the use of the inductor in the circuit is the way it is analyzed, i.e. if it is a differential inductor or an inductor with an AC grounded port. The scheme of Fig. 2.23 shows the way we perform the study, using the AC analysis. Considering a single-ended inductor, one of its ports is connected to the source and the other is grounded. For a differential inductor, its middle port is AC grounded and the other two are connected to identical sources with a phase difference of 180° in order to consider the differential voltages between these ports. With the latter analysis, its serial or parallel networks are found.

The inductor has a complex series impedance

$$Z_{ind} = R_{s,ind} + jX_{s,ind} = R_{p,ind} // jX_{p,ind} \tag{2.24}$$

where $R_{s,ind}$ and $R_{p,ind}$ are the parasitic series and parallel resistances and $X_{s,ind}$ and $X_{p,ind}$ are the series and parallel reactance, respectively. The reactances, divided by the angular frequency $\omega_0 = 2\pi f_0$, are the equivalent series and parallel inductance $L_{s,ind}$ and $L_{p,ind}$.

The inductor quality factor is defined as

$$Q_{ind} = \frac{X_{s,ind}}{R_{s,ind}} = \frac{R_{p,ind}}{X_{p,ind}} \tag{2.25}$$

The equivalent inductance of the parallel network is

$$L_{p,ind} = L_{s,ind}(1 + 1/Q_{ind}^2) \tag{2.26}$$

and the parasitic parallel resistance of the parallel network is

$$R_{p,ind} = R_{s,ind}(1 + Q_{ind}^2). \tag{2.27}$$

For real on-chip inductors with $Q_{ind} \geq 4$, $L_{p,ind} \cong L_{s,ind} = L_{ind}$.

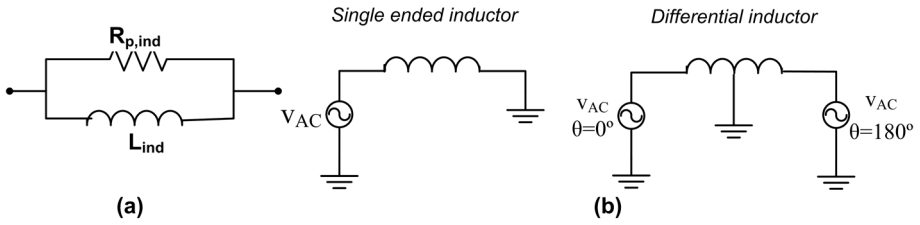


Figure 2.23: *(a) Parallel inductor modeling and (b) schematic of AC analysis for single-ended and differential inductors.*

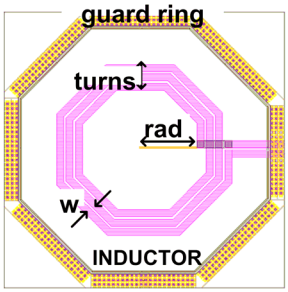


Figure 2.24: *Inductor layout and physical characteristics: coil widths, number of turns and radius.*

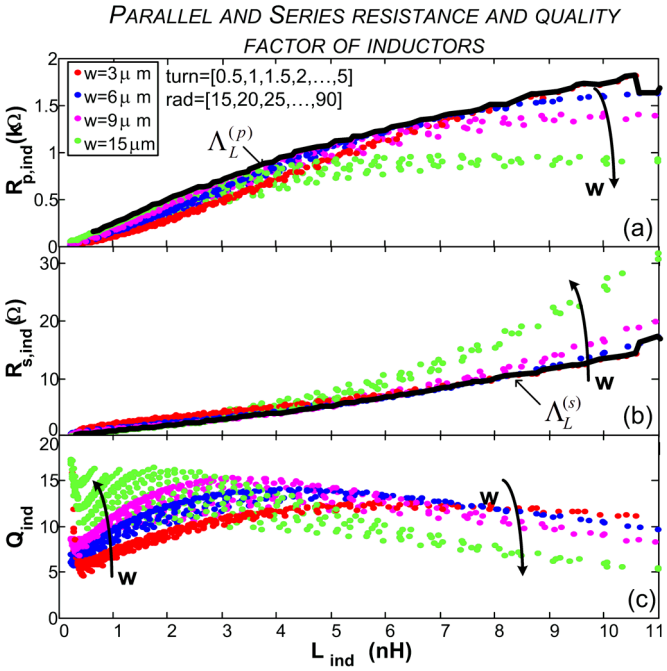


Figure 2.25: *(a) Parallel resistance, (b) series resistance and (c) quality factor versus L_{ind} for f_0=2.4 GHz, for four inductor widths, up to sixteen internal radius (rad) and up to 21 turns (turn). Maximum parallel resistance and minimum series resistance for each feasible inductance is marked with a black line.*

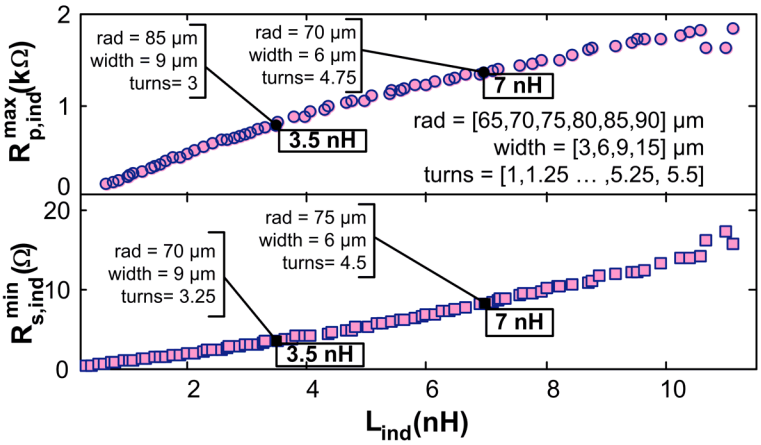


Figure 2.26: *Inductors LUTs: maximum parallel parasitic resistance and minimum series parasitic resistance for each feasible inductance in the reference technology.*

In these conditions the semi-empirical model of inductors contains $R^{min}_{s,ind}$ and $R^{max}_{p,ind}$ versus L_{ind} for a certain working frequency f_0, where $R^{min}_{s,ind}$ and $R^{max}_{p,ind}$ are the minimum $R_{s,ind}$ and maximum $R_{p,ind}$ for all the possible inductors of the technology. Considering these relations, the first step in the characterization of a set of technology inductors is to run the AC analysis for a large set of inductors, varying the inductor turns (turn), coil widths (w) and internal radius (rad) (which are shown in the layout of Fig. 2.24, in order to obtain a complete collection of modeled devices characteristics, i.e. $R_{s,ind}$, $R_{p,ind}$, Q_{ind} for L_{ind}.

For TECHNO1, the LUTs include the scatter plots of Fig. 2.25, when both coil inductor width, internal radius and number of turns are swept. The minimum quality factor Q_{ind} of the selected inductors is 5, to be far from the self resonance frequency of the device. The second step is to collect two inductor LUTs, $\Lambda^{(s)}_L$ and $\Lambda^{(p)}_L$, where for each inductance value, we get the lowest series and the highest parallel resistance, respectively, and the geometric aspect of its implementation. The results are displayed in the black lines of Fig. 2.25.(a) and (b), for $R_{p,ind}$ and $R_{s,ind}$, versus L_{ind}, and replotted separately in Fig. 2.26. The characterization has been made dense enough to cover the whole range of inductances with a logarithmic grid of 20 points per decade. This fact will be justified at the end of Section 4.1.3. The data in these plots show that for this technology the highest parallel resistances come with the largest inductor values whereas lowest serial resistance values correspond with low inductor values.

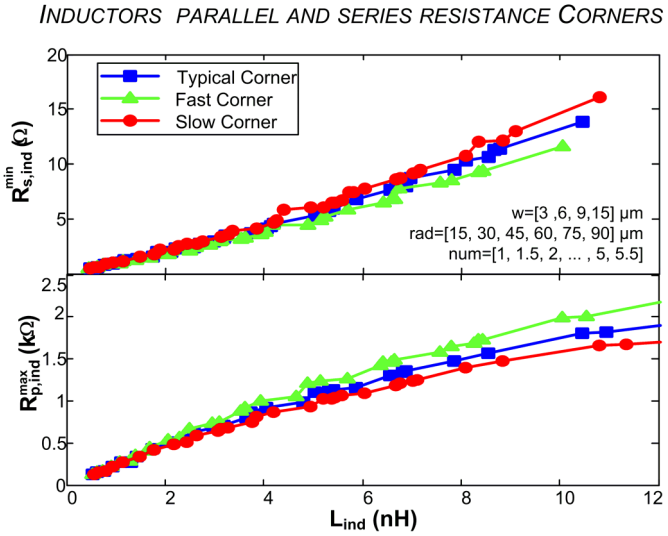


Figure 2.27: *$R^{min}_{s,ind}$ and $R^{max}_{p,ind}$ corners versus L_{ind} for f_0=2.4 GHz.*

Serial and parallel resistances as well as the inductances will change with technology variations. Here it is presented the process corners variations of the serial and parallel resistances versus L_{ind} in Fig. 2.27. Due to the slight change with the corners, it can be concluded that in a first approximation the corners cannot be taken into account in the variations of the designs characteristics.

2.3.2 Capacitor and varactor modeling

As well as inductors, we model the capacitors and varactors as AC serial or parallel networks, depending on their use in the circuit. Figure 2.28.(a) sketch the parallel network that model these devices. This network consists of a reactance in parallel with the parasitic resistance. It can be transformed into an AC serial network as

$$Z_{cap} = R_{p,cap}//-jX_{p,cap} = R_{s,cap} - jX_{s,cap} \tag{2.28}$$

where $R_{s,cap}$ and $R_{p,cap}$ are the serial and parallel parasitic resistances and -$X_{s,cap}$ and -$X_{p,cap}$ its series and parallel reactances. Then, the equivalent parallel capacitance $C_{p,cap}$ is

$$C_{p,cap} = 1/(2\pi f_0 X_{p,cap}). \tag{2.29}$$

where f_0 is the working frequency. The quality factor, Q_{cap} is

$$Q_{cap} = R_{p,cap}/X_{p,cap} = X_{s,cap}/R_{s,cap}, \tag{2.30}$$

thus, the relations between the series and the parallel resistances and capacitances are

$$R_{s,cap} = \frac{R_{p,cap}}{Q_{cap}^2 + 1}, \tag{2.31}$$

and

$$C_{s,cap} = C_{p,cap}\left(1 + \frac{1}{Q_{cap}^2}\right). \tag{2.32}$$

When $Q_{cap} \geq 4$ parallel and serial capacitances could be considered equal, i.e. $C_{p,cap} = C_{s,cap} = C_{cap}$.

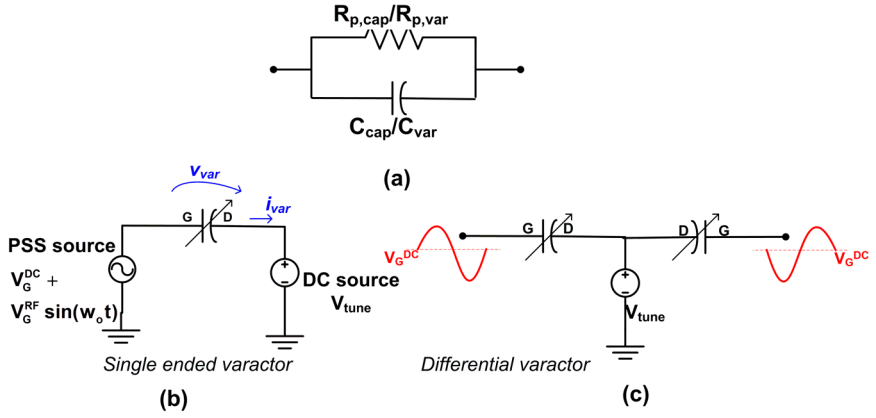


Figure 2.28: *(a) Parallel capacitor/varactor modeling. (b) Single-ended and (c) differential scheme of the varactor parameter extraction.*

The semi-empirical model includes in the LUTs C_{cap}, $R^{min}_{s,cap}$ and $R^{max}_{p,cap}$, where $R^{min}_{s,cap}$ and $R^{max}_{p,cap}$ are the minimum serial and maximum parallel resistances of the feasible technology capacitors. The same is applied for the varactors. As well as for the inductors, AC analysis is again utilized to characterize these components and generate the correspondent LUT, for capacitors with $Q_{cap} \geq 5$ to be far from the self resonance frequency of the device. The LUT collects $R_{p,cap}$, $R_{s,cap}$, Q_{cap} and C_{cap} as well as the capacitor dimensions for each capacitor sizing.

- **Capacitors**

This section briefly presents the features of the capacitors used in this thesis, the Metal-Insulator-Metal (MIM) capacitors, which layout is shown in Fig. 2.29. As well as the inductors, the first step in the characterization is to run an AC analysis for a considerable number of devices to collect their characteristics. Varying their width w and length l, we collect the data shown in Fig. 2.30, where the scattering plots cover w and l between 4 μm and 30 μm.

The second step is to collect two capacitor LUTs, $\Lambda^{(s)}_C$ and $\Lambda^{(p)}_C$, where for each capacitance value we extract the lowest series and highest parallel resistance, respectively. This step is graphically represented in the black lines of $R_{s,cap}$ and $R_{p,cap}$ versus C_{cap} of Fig. 2.30.(a) and (b).

These data show the very high quality factors of the MiM capacitors, above 50 for C_{cap} below 2 pF, and that the parallel/serial resistances are sufficiently high/slow in all cases. This leads us to make a simplification in the capacitor design used in this work, imposing a physical constraint over the capacitor sizing: w and l are equally set. We gain in design simplicity without loosing design quality. In Appendix 2.B the curves of $R_{s,cap}$, $R_{p,cap}$ and Q_{cap} versus C_{cap} for $w = l$ are presented.

From the corresponding plots some conclusions arise. Considering the serial parasitic resistance, it increases up to 6 Ω for very small capacitances and decreases to less than 1 Ω for capacitors higher than 1 pF, so if serial resistance is a strong

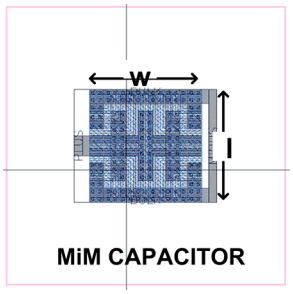


Figure 2.29: *Layout of the MiM capacitors, showing their width (w) and length (l) parameters.*

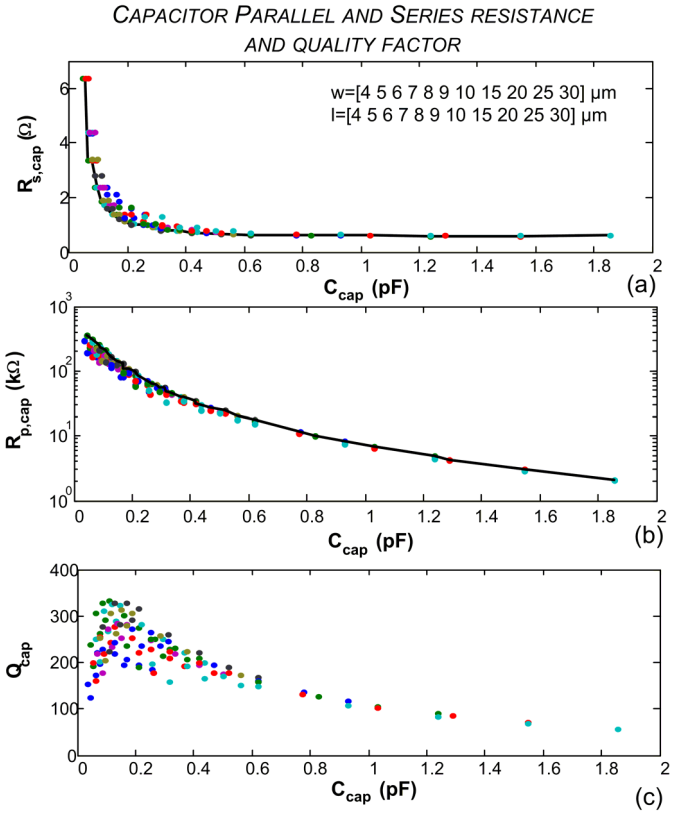


Figure 2.30: *MiM capacitors (a) serial and (b) parallel parasitic resistances and (c) quality factor versus C_{cap}, varying w and l.*

constraint in the design, very low capacitances could not be used. Next, when parallel parasitic resistance is studied, it is observed that small capacitors have very high resistances (higher than 300 kΩ), whereas for high capacitances those values fall down to 2 kΩ. Then, for designs where high parallel resistance values are compulsory, there are maximum values of w and l above which the capacitors cannot be used. The capacitance quality factor Q_{cap} have values over the hundred for C_{cap} below 1 pF and over fifty for C_{cap} between 1 pF and 2 pF.

To complete this study we present the simulations for typical, slow and fast corners for $R^{min}_{s,cap}$ and $R^{max}_{p,cap}$. The results are resumed in Fig. 2.31. For low values of C_{cap} (below 200 fF) the spread of $R^{max}_{p,cap}$ and $R^{min}_{s,cap}$ is noticeable. However, this variation does not reduce enough the parallel resistance (or dows not increase the serial resistance) to make them have a very low quality factor; meaning that the spread due to the corners for low capacitor values is not important. For high capacitor values, the spread is mainly in the resulting capacitance - as shown with the bubble of Fig. 2.31.(c)-, and would modify the design results.

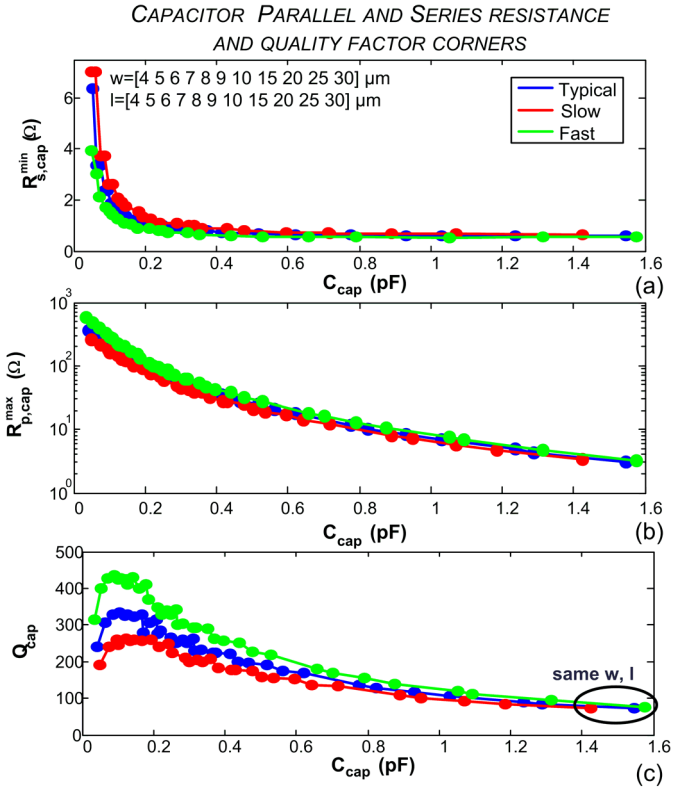


Figure 2.31: *Corner simulations results for: (a) $R^{min}_{s,cap}$, (b) $R^{max}_{p,cap}$ and (c) Q_{cap} vs C_{cap} for f_0=2.4 GHz.*

The low serial and high parallel resistances, as well as the high quality factors of these capacitors permit considering the MIM capacitors as almost-ideal devices, in comparison with inductors or transistors. It appreciably simplifies the circuit design and the creation of design methodologies, as we will see later on. Therefore, for very high-Q values (above 50), the capacitors are considered as ideal in this thesis.

• **Varactors**

Varactors are generally based on semiconductor devices and have much lower quality factor than MiM capacitors. In this work, both TECH1 and TECH2 provide MOS accumulation varactors. Their quality factors could be comparable with the ones of high-Q on-chip inductors. Also their parasitic resistances suffer from variations when the tuning voltage V_{tune} (at the drain-source terminal), the DC voltage V_G^{DC} and the amplitude voltage V_G^{RF} at the gate, changing the effective capacitance [Hega 03]. As a result, a study should be done for different design conditions. As varactors are very dependent on the signal amplitudes, it is not always possible to use a AC analysis as it is a small-signal analysis. For these devices, we need a large-signal analysis, and in this case we utilize the PSS analysis of the SpectreRF simulator of CADENCE. It enables us to calculate the impedance Z_{var} seen between the terminals G-D/S at the working frequency f_0, i.e. $Z_{var} = \underline{V}(f_0)/\underline{I}(f_0)$, where $\underline{V}$ and $\underline{I}$ are the phasors in f_0 of v_{var} and i_{var} of Fig. 2.28.(b). This way we obtain the effective serial resistance $R_{s,var}$, the effective parallel resistance $R_{p,var}$ and capacitance C_{var} at the working frequency. As in this dissertation we only use the varactors in the VCO design (Chapter 3), this study is only focused on this particular application; V_{tune} is fixed to 0.5 V (in the middle of its range), V_G^{RF} is set to 400 mV and V_G^{DC} is fixed to 500 mV, which are representative voltages in the VCO implementation.

As well as the inductor or capacitor previous approaches, the serial network is initially used to characterize a varactor. Their serial resistance and equivalent capacitance are, respectively, $R_{s,var}$ and C_{var}. Again, it is possible to transform this network into a parallel one, utilizing the expressions (2.31) and (2.32). Figure 2.28.(b) and (c) show the employed data extraction scheme for varactors.

In this thesis, single-ended varactors are not used stand-alone; instead, only varactors in the differential configuration are implemented, as shown in Fig. 2.28(c). As the differential architecture is formed by two single-ended varactors and, as their drain voltage is ideally fixed to a V_{tune} value, this study of single-ended varactors is still valid here.

The first step is to collect the features of a considerable amount of devices. The varactors of TECH1 have a fixed finger of W/L=1.6 μm/400 nm, and the designer can sweep both the number of fingers fng and the number of rows of these fingers grp (as shown in Fig. 2.32). In this study fng={1,4,8,16,32} and grp is swept from 1 to 16. The results of $R_{s,var}$, $R_{p,var}$ and Q_{var} versus C_{var} are presented in Fig. 2.33.

The second step is to collect two varactors LUTs, $\Lambda_V^{(s)}$ and $\Lambda_V^{(p)}$ for the lowest series and largest parallel resistance for each feasible effective capacitance. The corresponding results are shown in Fig. 2.33.(a) and Fig. 2.33.(b) with square symbols.

Figure 2.34 shows the variation in the LUT varactor characteristics ($\Lambda_V^{(s)}$ and

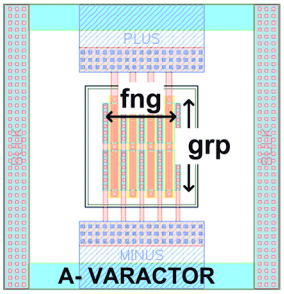


Figure 2.32: *Layout of the varactors of TECH1, showing the involved parameters fng and grp.*

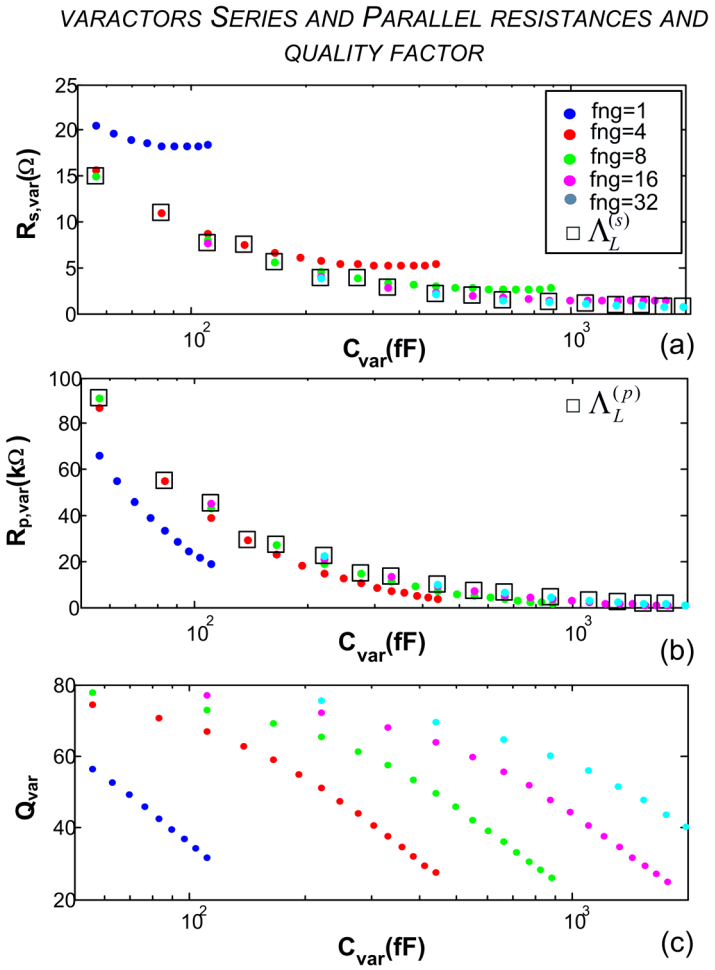


Figure 2.33: *(a) $R_{s,var}$, (b) $R_{p,var}$, (c) Q_{var} versus C_{var}. The squared markers shows (a) the minimum series and (b) maximum parallel parasitic resistances.*

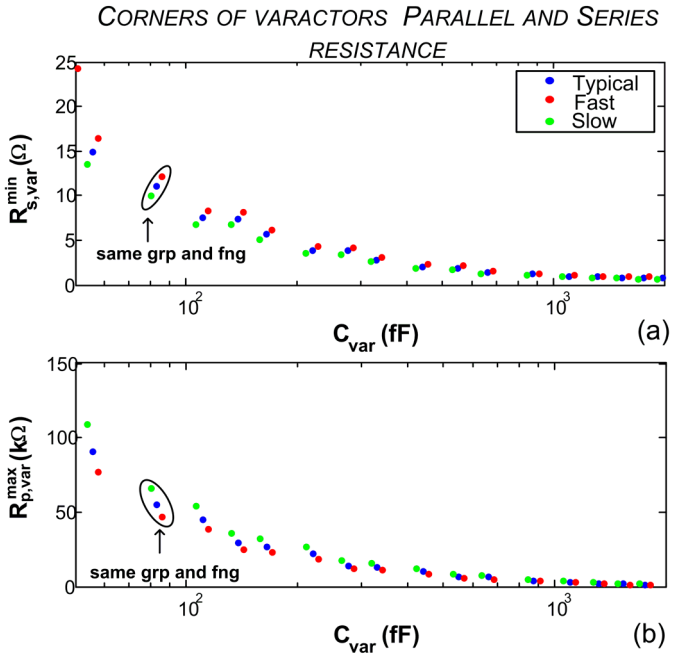


Figure 2.34: *(a) $R^{min}_{s,var}$ and (b) $R^{max}_{p,var}$ versus C_{var} for f_0=2.4 GHz.*

$\Lambda_V^{(p)}$) for typical, fast and slow corners. The maximum spread is 17 Ω for the $R^{min}_{s,var}$ and 15 kΩ for the $R^{max}_{p,var}$ for low capacitance values, which is acceptable for the absolute parasitic values of the varactors.

2.3.3 Resistor modeling

In this section there are only studied resistors with low resistances values. The reason is that they would be used to adjust the input or output impedances of RF circuits, as LNAs. Applications that include high resistances are not considered in this thesis, so modeling these elements are out of the scope of this study. The technologies used have several types of integrated resistors but we only discuss here the characteristics of the RF characterized P+ Poly resistors with silicide, which are appropriate when low resistance values are needed in RF. The model presented here is used only when the resistor is in an RF path.

As well as inductors and capacitors, integrated resistors have associated parasitics, and therefore, we could model it accordingly with an AC analysis. Depending on the resistor type and size, its equivalent parasitic in AC could be capacitive or inductive. As the monolithic resistors studied have low resistance values, it is more convenient to model them as a resistor R_{res} in series with a series reactance $X_{s,res}$, as shown in Fig. 2.35 with its correspondent quality factor Q_{res}, defined as

$$Q_{res} = \frac{R_{res}}{|X_{s,res}|}. \tag{2.33}$$

The semi-empirical model of the resistor includes $X^{min}_{s,res}$, which is the minimum $X_{s,res}$ for each feasible resistor value of the technology and the correspondent R_{res}.

The resistance of the P+ Poly resistors with silicide is set fixing their width w and length l. In this work the width is swept from 2 μm to 10 μm despite it can be further reduced to less than 0.5 μm. Is is done in order to position at least 6 contacts in each resistor's terminal to reduce the equivalent contact resistance. Then, the study is done performing an AC analysis for $l \in [2 \times w, 150\ \mu m]$ and $w = 2,3,5,8,10$ μm. This first step in the characterization is to collect the device characteristics R_{res}, $X_{s,res}$ and Q_{res}, as it is shown in the scattered plots of Fig. 2.36.

The second step is to collect the resistor LUT $\Lambda^{(s)}_R$, where for each resistance value it is found the lowest $|X_{s,res}|$, and the geometric sizing of each implementation. These values are highlighted in Fig. 2.36.(a) with the square symbols.

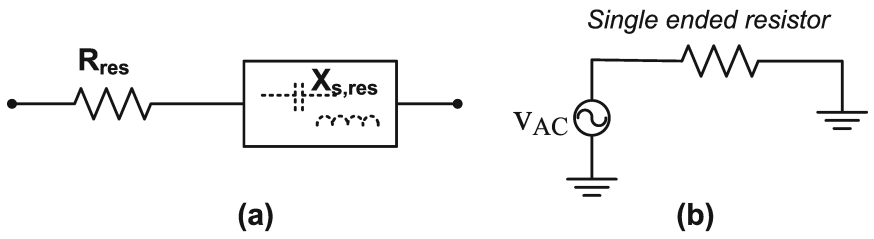


Figure 2.35: *(a) Series resistor model, where the reactance can be capacitive or inductive, and (b) AC simulation scheme.*

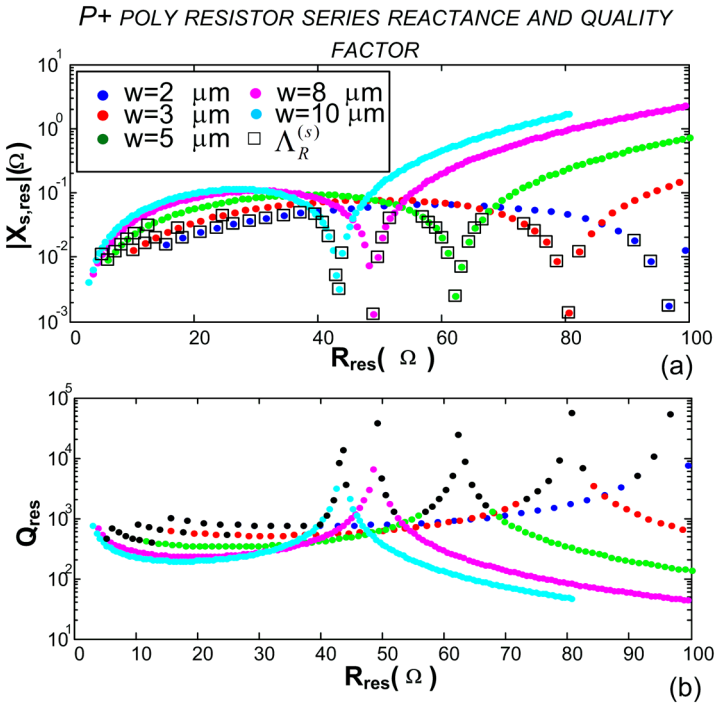


Figure 2.36: *P+ Poly resistor characteristics:(a) $X_{s,res}$ vs R_{res}, (b) Q_{res} vs R_{res}, for f_0=2.4 GHz.*

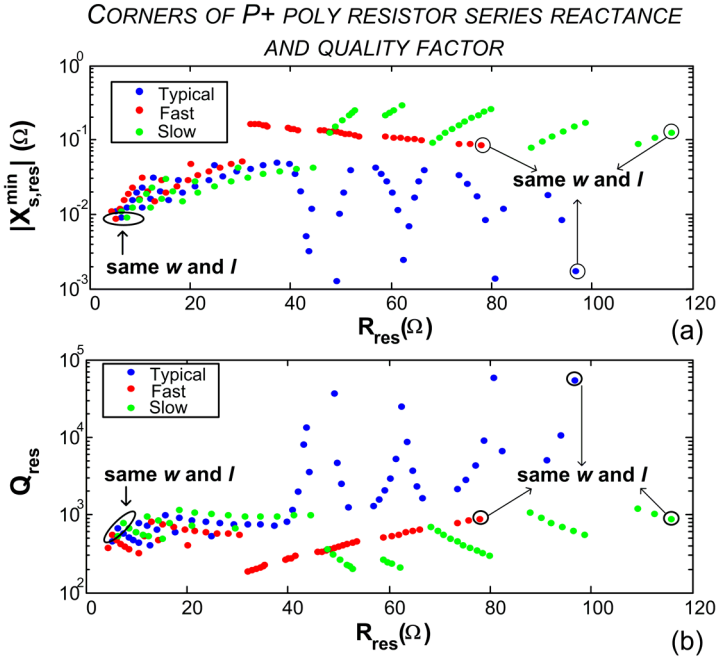


Figure 2.37: $X_{s,res}^{min}$ *corners versus* R_{res}.

Finally, to study the variations in the resistor characteristics we present the results of the typical, fast and slow corners for the optimum resistances (represented by square symbols of Fig. 2.36.(a)) in Fig. 2.37. In the plot it is highlighted the spread of the reactance and quality factor values when the corner changes for two cases, low and high resistances. $|X_{s,res}|$ are always below 1 Ω and Q_{res} always above 100, so these variations will not be appreciable in the circuit behavior.

2.4 Conclusions

In this chapter we presented the implementation of the first two steps of the design methodology of Chapter 1, including the semi-empirical models adopted for all the devices used in the design methodology. We review the MOS transistor model for all-inversion regions, studying the curve g_m/I_D versus i and the behavior of f_T when the bias point moves from weak inversion to strong inversion region. We show the importance, already highlighted by other works, of working with a MOS transistor model that covers all-inversion regions of operation and therefore exploiting to its maximum the MOS transistor potential and the performance trade-offs. We show that for RF circuits integrated in nanometer technologies, the best trade-off occurs in many cases in the moderate region.

We study the behavior of the transistor characteristics g_m/I_D ratio, g_{ds}/I_D ratio, g_{ds}, $C_{ij}^{'}$, V_{OD} and noise parameters for changes in the size,the drain voltage or the technology characteristics in order to know the limitations of the last two steps of the general design methodology.

Finally, an analysis of the main passive components of an RF design as inductors, capacitors and resistors is also developed, evaluating for a typical nanometer RF CMOS technology its modeling, its parasitics and quality factors, and the variations with corners.

2.A Appendix A: MOST parameters as function of i

To study the behavior of f_T with g_m/I_D, Fig. 2.38 plots, in blue and in green, the f_T and g_m/I_D versus i, respectively, for nMOS W_n and n_f, where it is clearly appreciated the reduction of f_T for moderate and weak inversion.

The characteristics of g_{ds}/I_D versus i for various transistor widths are visualized in Fig. 2.39. When narrow devices are not considered, no significant spread in the curve is observed.

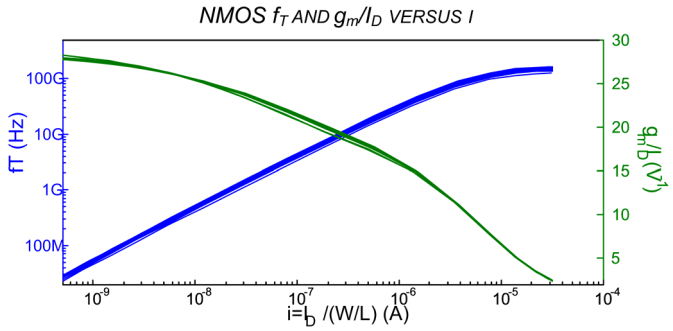


Figure 2.38: *nMOS transistor transition frequency f_T and g_m/I_D vs. i for the technology TECH1.*

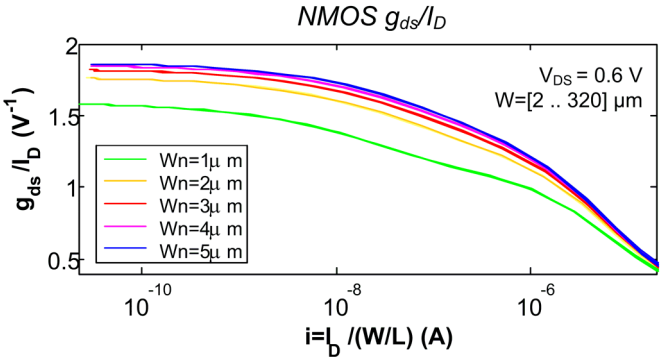


Figure 2.39: g_{ds}/I_D *vs. i for TECH1.*

2.B Appendix B: Maps of capacitors obtained with $w = l$

As discussed in this chapter the physical constraint for MiMs of $w = l$ is considered in the rest of the work. Therefore, sweeping w=l and applying the electrical AC analysis, the data of serial, and parallel resistances and capacitances are collected. Then, fixing this constraint, a look-up table is obtained, in which for each w, and therefore each C_{cap}, exists a one-to-one relation with a $R_{s,cap}$, $R_{s,cap}$ and C_{cap}. These relations are shown in Fig. 2.40.(a), (b) and (c), where the serial resistance $R_{s,cap}$, parallel resistance $R_{p,cap}$ and quality factor Q_{cap} versus C_{cap} are visualized.

Finally, for $w = l$, the corners for $R_{s,cap}$, $R_{p,cap}$ and Q_{cap} are visualized in Fig. 2.41. The spread in the parasitic resistances and the quality factor is not substantial as the serial/parallel parasitic resistance are maintained low/high.

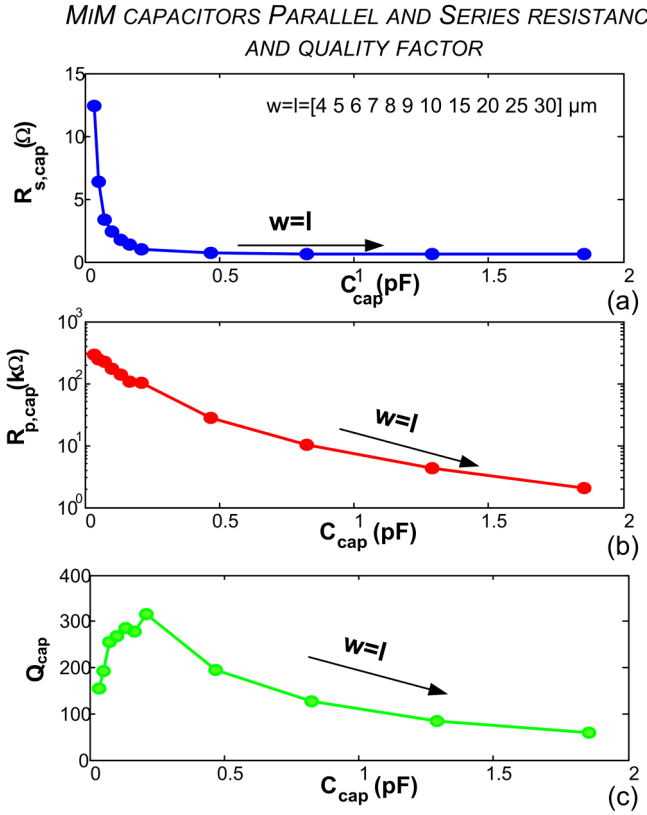


Figure 2.40: *(a) Serial resistance, (b) parallel resistance and (c) quality factor versus serial capacitance for MIM capacitors with equal width and length, for f_0=2.4 GHz.*

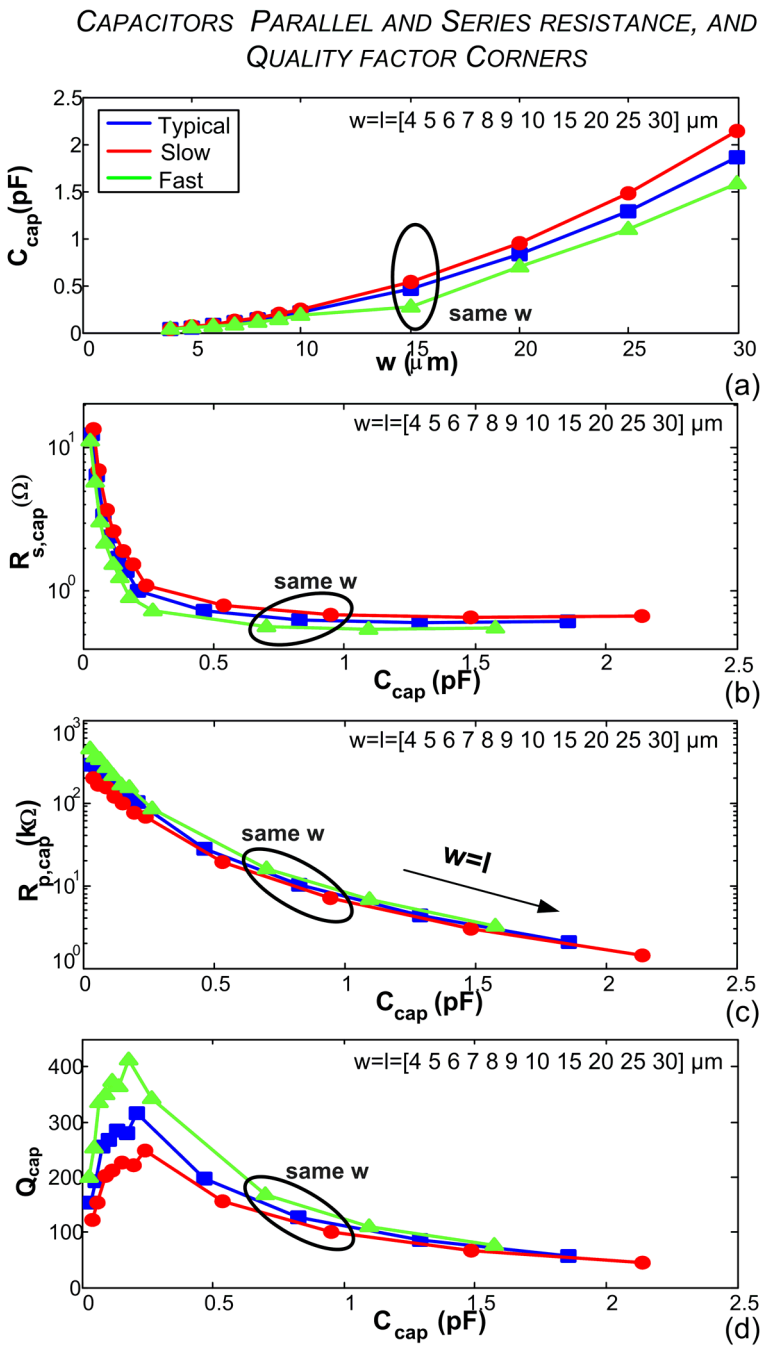


Figure 2.41: *Corner simulations for: (a) C_{cap} versus w; (b) $R_{s,par}$, (c) $R_{p,cap}$ and (d) Q_{cap} versus C_{cap}, for f_0=2.4 GHz.*

2.C Appendix C: TECH2 technology characteristics

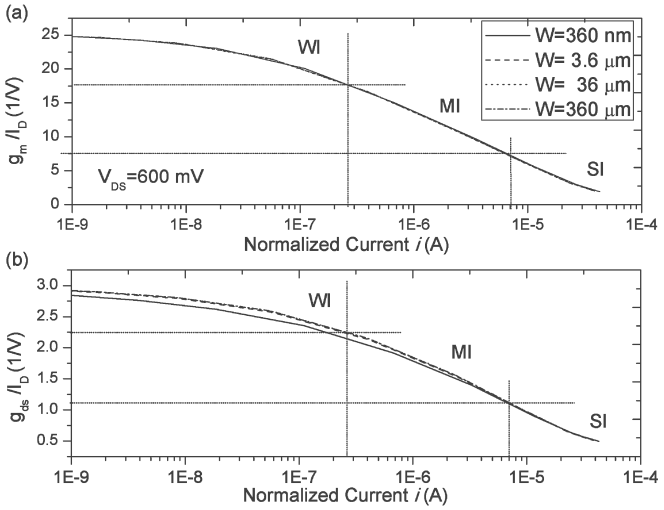


Figure 2.42: *(a) g_m/I_D and (b) g_{ds}/I_D vs. $i = I_D/(W/L)$ for four nMOS transistors and a $V_{DS} = 600\ mV$. Typical limits of strong (SI), moderate (MI) and weak (WI) inversion regions are shown.*

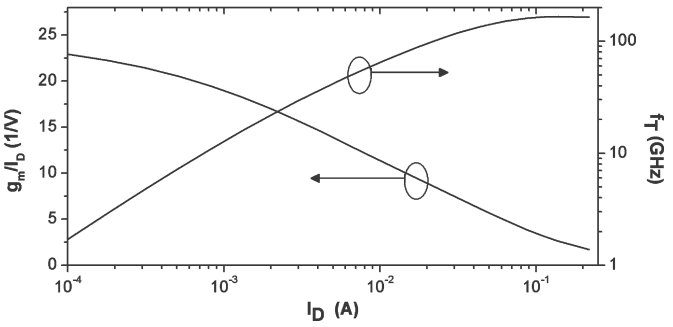


Figure 2.43: *g_m/I_D and f_T versus I_D of a pMOS transistor with an aspect ratio of 360 μm/100 nm.*

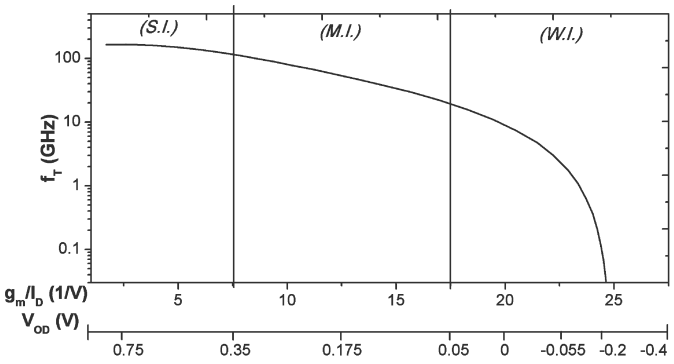


Figure 2.44: *f_T versus g_m/I_D and versus the overdrive voltage V_{OD} for nMOS transistors.*

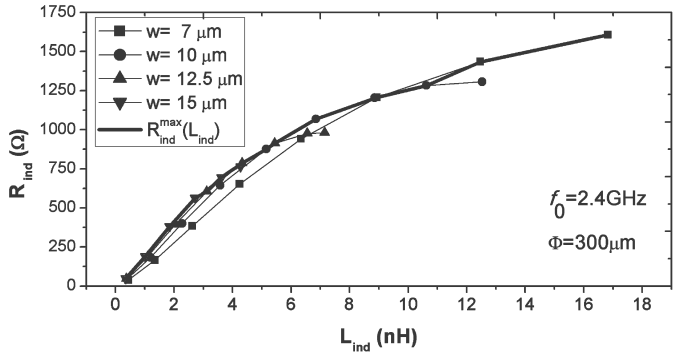


Figure 2.45: *Parallel resistance versus L_{ind} for four inductor coil widths w with a common external diameter of 300 μm, at f_0=2.4 GHz. The black line represents the inductors with the highest resistance.*

CHAPTER 3

VCOs design methodology

THE IMPLEMENTATION OF THE TWO LAST steps of the design methodology for the inductor-capacitor-tank voltage controlled oscillators (LC-VCOs), is discussed in this chapter. The motivation of this study on VCOs is the fact that these circuits, due to their phase noise, are responsible for most part of the error in the processed signal in an RF receiver [Leen 01], as well as for a significant percentage of the system current consumption. The design methodology presented here optimizes the VCO design by means of exploiting the consumption-spectral purity trade-off of the VCOs in order to use just the needed current to fulfill the application requirements. This is achieved by using the transconductance to drain current ratio g_m/I_D tool presented in Chapter 2 and by taking advantage of the MOS transistor operation in all-inversion regions.

To prove the flexibility of our methodology, two VCO architectures are considered here. First, the complementary cross coupled differential LC-VCO architecture, shown in Fig. 3.1.(a) and studied in Sections 3.2 and 3.3. Then, the all-nMOS (or all-pMOS) cross-coupled VCO architecture is revised, depicted in Fig. 3.1.(b), and discussed in Section 3.4.

Considering the complementary cross-coupled differential LC-VCO, two approaches were considered. A simplified approach fixes the transconductances of pMOS and nMOS transistors as equal, and a general approach lifts this limitation and permits both transconductances taking different values.

For each architecture, the VCO behavior is described analytically by means of a set of equations, in order to implement the third step of the methodology guidelines of Section 1.1. Whenever possible, the LC-VCO expressions are reformulated to include the g_m/I_D ratio. To complete the design methodology, the VCO design flows and the study of design maps and application examples resulting from the computations are generated. Design flows are proposed based on the VCO equations set, the extracted characteristics of the MOS transistor (i.e. g_m/I_D ratio vs i, g_{ds}/I_D and C'_{ij} vs. g_m/I_D), the inductors ($R_{p,ind}$ and L_{ind}) and the varactors. These design flows obtain the sizing of the VCO components for a set of constraints that include power consumption, phase noise and voltage swing.

Design space exploration for each approach, utilizing the 90nm CMOS TECH2 technology, have been obtained. In order to study the compromises arisen from working in weak, moderate or strong inversion, four design points are chosen and

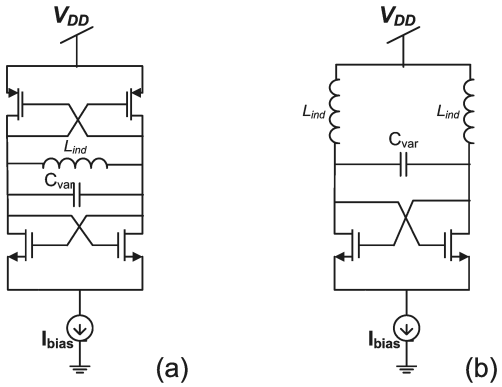


Figure 3.1: *(a) Differential cross-coupled and (b) all-nMOS LC-VCOs*

quantitatively compared. Finally, one of these design points is utilized to fabricate an LC-VCO, whose final implementation and measurements are exposed in this chapter. This implementation help us to verify the phase noise model and the proposed design methodology.

For the phase noise expressions needed to do the computations we develop an all-inversion region phase noise model for the white noise and flicker noise zones based on the Hajimiri and Lee's phase noise model presented in [Haji 98]. It is provided the phase noise modeled in the $1/f^2$ and $1/f^3$ zones.

This chapter is organized in the following way. First, a review of previous works on LC-VCO optimization techniques is presented in Section 3.1. Next, in Section 3.2, the LC-VCO simplified approach is considered, presenting the signal modeling, the phase noise modeling for all-inversion regions, the design flow, the validation by simulations and the experimental validation through a fabricated LC-VCO in moderate inversion. Afterwards, Section 3.3 introduces the general approach, including the new signal modeling, and phase noise modeling and the proposed design flow. Then Section 3.4 discusses the methodology for all-nMOS/all-pMOS LC-VCOs. Finally, comes the chapter's conclusions.

3.1 Review of LC-VCO optimization techniques

From the hundreds of published works that present the design of LC-VCOs, few of them present a deep study of the design techniques used. It is due to the difficulty in describing all the LC-VCO features in an analytical way. From the published works that present their design techniques, the majority is focused on reducing the phase noise as the papers of Hajimiri and Lee [Haji 99], Jia et al [Jia 05], Kao and Hsu [Kao 05] and Mellouli et al.[Mell 11]. The work of Hajimiri and Lee uses the phase noise theory presented by the authors in [Haji 98], analyzing the VCO phase noise, and studying the phase noise characteristic versus the supply voltage and the tail current. However this work does not present the rest of VCO expressions used in the design. A similar approach is followed by Kao and Hsu. It is not the case of the work of Jia et al., which includes all the equations involved as well as a discussion of possible sizing of the MOS transistors of the VCO.

Other authors present a global optimization methodology where phase noise, power consumption, tunning and/or voltage amplitude, among others, are included in the optimization flow. These works are much more useful for a designer as in a real VCO design not only the phase noise matters. This is the case of the works of Ham and Hajimiri [Ham 01, Ham 02] or of De Ranter et al. [De R 02]. The works of Ham, Hajimiri, Melloulli or De Ranter utilize graphical methods to perform the methodologies, which help the designer in positioning in the design space and observe the involved trade-offs. De Ranter et al. perform the VCO sizing and layout automatically, providing a ready-to-use VCO at the end of the process. The difficulty of their approach is to have correct cost-functions for all the VCO features.

Considering the use of MOS transistor analytical equations, the works of Ham or Jia present MOS transistor analytical equations, but only working in strong inversion region. The works of Perumana [Peru 08] and Lee and Mohammadi [Lee 07] use the subthreshold regime, by means of the I-V exponential equation, in the design of the receiver blocks, but does not provide a thorough description of the VCO design methodology.

Our works presents a design methodology based on the analytical description of the VCO, the use of all-inversion-regions, the g_m/I_D tool and the graphical method to observe the VCO trade-offs. The first approach of our methodology was made in [Fior 09], where the initial considerations of the design methodology as well as the design of a moderate inversion VCO in AMS 0.35μm technology are presented. The advances of our study were published in [Fior 11a] and [Fior 12] and they are fully discussed in this chapter.

3.2 Cross-coupled differential LC-VCO: simplified approach

3.2.1 Signal Modeling

This section presents the set of equations and the design flow that describe the cross coupled complementary LC-VCO, in a simplified approach in which nMOS and pMOS transistors are sized so that their transconductances, $g_{m,p}$ and $g_{m,n}$, match, i.e. $g_{m,n} = g_{m,p} = g_m$.

A detailed view of a differential cross coupled LC-VCOs is depicted in Fig. 3.2; it shows the complementary VCO with its LC tank ($L_{ind}//C_{var}$), biased with a pMOS current mirror, which drives the I_{bias} current to the VCO core. This pMOS structure is chosen here for its better flicker noise performance with respect to an nMOS one with the same size [O 02]. Cross-coupled transistors (M_n, M_p) provide the needed negative feedback and the pMOS-nMOS complementary structure increases the equivalent VCO transconductance while consuming the same quiescent drain current, I_D, with $I_{bias} = 2 \cdot I_D$.

The fully-differential small-signal model of the LC-VCO of Fig. 3.2 is displayed in Fig. 3.3.(a) jointly with its reduced model in Fig. 3.2.(b). It comprises

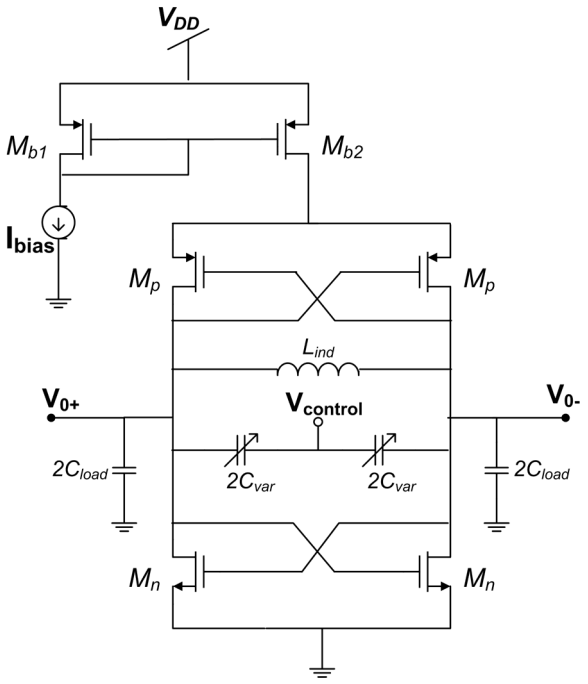


Figure 3.2: *Cross coupled complementary LC-VCO.*

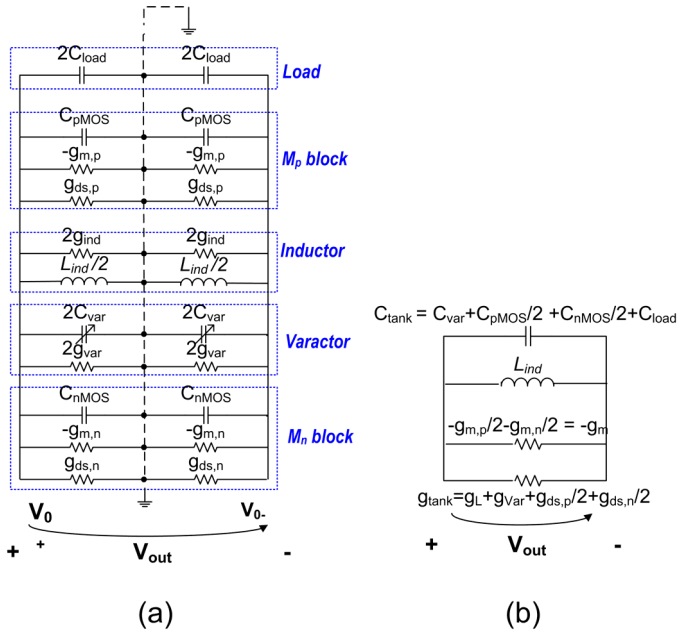


Figure 3.3: *Small signal LC-VCO model:(a) a complete model and (b) a reduced model.*

the equivalent inductance of the differential inductor L_{ind} and the equivalent capacitance of the varactors C_{var} jointly with its parasitic parallel conductances g_{ind} and g_{var}, respectively; the equivalent parasitic capacitances C_{nMOS} and C_{pMOS}, the conductances $g_{ds,n}$ and $g_{ds,p}$ and transconductances $g_{m,n}$ and $g_{m,p}$ of the nMOS and pMOS transistors; and the load capacitance C_{load}.

Now, considering C_{tank} and g_{tank} as the equivalent capacitance and parallel conductance of the VCO tank, respectively, the well-known oscillation frequency f_0 and oscillation condition expressions are, respectively [Ham 02]

$$f_0 = \frac{1}{2\pi\sqrt{L_{ind}C_{tank}}} \tag{3.1}$$

and

$$g_{tank} \leq \frac{g_{m,p}}{2} + \frac{g_{m,n}}{2} \tag{3.2}$$

As $g_{m,n} = g_{m,p} = g_m$, (3.2) simplifies to

$$g_{tank} \leq g_m \tag{3.3}$$

Studying Fig. 3.2.(b) and grouping the components capacitances and conductances of the tank into C_{tank} and g_{tank}, we obtain that

$$C_{tank} = C_{var} + \frac{C_{pMOS} + C_{nMOS}}{2} + C_{load} \tag{3.4}$$

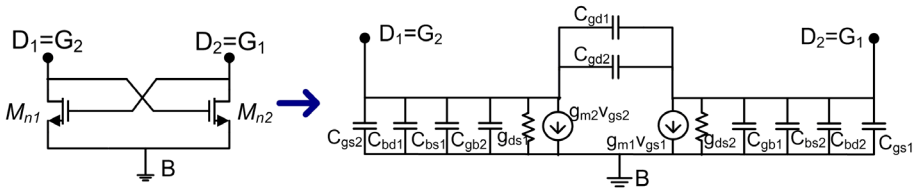


Figure 3.4: *Quasiestatic simplified model of the cross-coupled structure.*

and

$$g_{tank} = g_{ind} + g_{var} + \frac{g_{ds,p}}{2} + \frac{g_{ds,n}}{2} \tag{3.5}$$

where $g_{ds,n}$ and $g_{ds,p}$ are the output conductances of the nMOS and pMOS transistors, g_{ind} inductor parasitic parallel conductance and g_{var} is the parasitic conductance of the varactor.

For the quasistatic MOS transistor model of five capacitances, the equivalent cross-coupled transistor capacitance C_{MOS}, valid both for the nMOS and pMOS transistors and presented in Fig. 3.4, is

$$C_{MOS} = 4C_{gd} + (C_{gs} + C_{gb} + C_{bd} + C_{bs}). \tag{3.6}$$

Due to the expected technology parameter variations, a safety margin factor k_{osc} -usually called oscillation factor- is utilized in (3.3) to transform the inequality into

$$g_m = k_{osc}\ g_{tank} \tag{3.7}$$

where k_{osc} is generally in the range of 1.5 to 3.

Using in (3.5) the MOST intrinsic gain A_i, defined as the gain of a common source transistor amplifier loaded by an ideal current source [Silv 96]

$$A_i = g_m/g_{ds} = \frac{g_m/I_D}{g_{ds}/I_D}. \tag{3.8}$$

we have

$$g_{tank} = g_{ind} + g_{var} + \frac{1}{2}\left(\frac{g_{m,p}}{A_{i,p}} + \frac{g_{m,n}}{A_{i,n}}\right) = g_{ind} + g_{var} + \frac{g_m}{2}\left(\frac{1}{A_{i,p}} + \frac{1}{A_{i,n}}\right). \tag{3.9}$$

that substituting in (3.7) and working out g_m, results the VCO oscillating condition

$$g_m = k'_{osc}(g_{ind} + g_{var}) \tag{3.10}$$

where

$$k'_{osc} = \left(\frac{1}{k_{osc}} - \frac{1}{2A_{i,p}} - \frac{1}{2A_{i,n}}\right)^{-1}. \tag{3.11}$$

If g_{var} is negligible with respect to g_{ind}

$$g_m = k'_{osc}\ g_{ind}. \tag{3.12}$$

The assumption of $g_{var} << g_{ind}$ must be checked during the design. As it will be shown latter on, this will simplify the design flow. Finally, the differential output voltage amplitude of the tank A_{out} is estimated as in [Haji 99]

$$A_{out} = max|V_{0+} - V_{0-}| \cong \frac{4}{\pi}\frac{2I_D}{g_{tank}} = \frac{8}{\pi}\frac{k_{osc}}{g_m/I_D}. \tag{3.13}$$

The intuitive idea which lays behind of this expression is the fact that when the VCO oscillates, the LC tank resonates, being its impedance purely resistive, and in each semi-period, the I_{bias} current switches to one of the circuit branches while the other branch is cut-off, flowing through the tank resistance. As only the fundamental voltage term of the square signal remains after tank filtering, it is immediate to see why the coefficient $4/\pi$ comes out.

The quiescent DC output voltage $V_{out}^{DC,Q}$ (when the VCO is not oscillating) is the gate-source voltage of the nMOS transistors and it is determined by using the V_{OD} voltage of the nMOST LUTs presented in Chapter 2. This value gives an idea of the DC output voltage V_{out}^{DC} when the VCO oscillates.

3.2.2 Phase noise modeling for all-inversion-regions

Now on, phase noise expressions for the cross-coupled LC-VCO are deduced considering all the inversion regions of the MOS transistor. These expressions contemplate separately the $1/f^3$ and $1/f^2$ asymptotic phase noise zones.

The phase noise $\mathcal{L}$ is the essential characteristic of any VCO; it describes its spectral purity around its oscillation frequency f_0 [Haji 98]. When an ideal oscillator is modeled, its output voltage can be expressed as

$$V_{out}(t) = A_{out}cos\big(\omega_0 t + \phi\big) \tag{3.14}$$

with constant values of amplitude A_{out} and phase ϕ. Then, ideally, the output spectrum of the VCO are two impulses at frequencies $\pm f_0$. However, when using a real oscillator, the amplitude and the phase are affected by noise and are time-variant, as follows

$$V_{out}(t) = A_{out}(t)cos\big(\omega_0 t + \phi(t)\big) \tag{3.15}$$

where $\phi(t)$ is called the excess phase of the output. The spectrum of this signal has sidebands close to f_0. These instabilities in amplitude and phase can be characterized by quantifying the single sideband noise spectral density around the carrier f_0 as following:

$$\mathcal{L}(\Delta f) = 10\ log\frac{P_{sideband}(f_0 + \Delta f, 1Hz)}{P_{carrier}} \tag{3.16}$$

where $P_{sideband}(f_0+\Delta f, 1Hz)$ is the single sideband power at a frequency offset Δf from the carrier, measured within a bandwidth of 1 Hz, and $P_{carrier}$ is the power of the signal at f_0. This noise characterization includes the effect of both amplitude and phase fluctuations, which is a disadvantage because it is not possible to know them separately. On the other hand, this parameter is easily measurable via a spectrum analyzer. In this work, it is assumed that the amplitude noise effect is almost eliminated due to the amplitude-limiting oscillator's mechanism of the VCO under study. So, the remaining noise is the phase noise, then (3.16) is considered to be the usual definition of phase noise.

It has been observed that, around f_0, three asymptotic zones can be defined [Lees 66]. Very near f_0, $\mathcal{L}$ decreases proportionally to $1/f^3$ and it is directly related to the flicker noise of MOS transistors. Then, a spectrum zone inversely proportional to f^2 appears, mainly caused by the white noise of VCO elements. Finally, far from f_0, there is a flat zone, the VCO noise floor, where the external noise sources dominate. In this work it is the $1/f^2$ zone where the VCO phase noise is specified, but this could be used for close-in phase noise. The asymptotic limits of the three regions can be found making equal the expressions for two adjacent zones and solving for f. Particularly, the flicker corner frequency $f_{c,1/f^3}$ is the VCO parameter that defines the lowest limit of the $1/f^2$ zone.

To visualize and fully exploit the phase noise-current consumption trade-off, an analytical model for phase noise valid for all-inversion regions is derived in this thesis by means of expressing the phase noise equations as functions of the g_m/I_D ratio. The initial expressions of this phase noise model were presented by Hajimiri and Lee in [Haji 98, Haji 99, Lee 00]. This is a linear time variant model, with compact equations, very suitable for our methodology. For the $1/f^2$ zone, the phase noise is

$$\mathcal{L}_{1/f^2}(\Delta f) = 10\ log\Big(\frac{\Gamma_{rms}^2 \overline{i_w^2}}{2q_{max}^2 \Delta f^2}\Big) \tag{3.17}$$

with Γ_{rms} the root-mean square value of the periodical function $\Gamma(\cdot)$ defined by Hajimiri as the sensitivity function from charge impulse to phase change in the VCO, q_{max} is the maximum charge at the equivalent tank capacitance and $\overline{i_w^2}$ is the white noise psd of the device. For the flicker noise zone, the expression is

$$\mathcal{L}_{1/f^3}(\Delta f) = 10\ log\Big(\frac{\overline{i_{1/f}^2}\Gamma_{avr}^2}{2q_{max}^2 \Delta f^2}\Big) \tag{3.18}$$

with $\overline{i_{1/f}^2}$ the flicker noise psd of the device and Γ_{avr} the average value of $\Gamma(\cdot)$. In Appendix 3.A it is presented a complete deduction of these equations [Haji 98].

3.2.3 $1/f^2$ region phase noise

To evaluate in all-inversion regions the phase noise expression for the cross-coupled differential LC-VCO, lets obtain the expressions of each component of (3.17). To do this study, the most important VCO white noise sources are obtained. For simplicity, it has been considered that no correlation exists between them. Then, superposition will be applied when substituting each noise source formula in (3.17).

The general expression of MOST white noise power spectral density, is given in (2.20). As a first approximation, the induced gate noise is discarded here, because we will assume that noise around the carrier frequency is governed principally by the baseband noise due to the upconversion mechanisms of the VCO. It is because of c_n coefficients of $\Gamma(\cdot)$ decrease as n grows, being generally c_0 the term of highest weight -the baseband coefficient- and then c_1. Then, the effect of radio-frequency noise is reduced, as it is the case of the induced gate noise.

Figure 3.5 depicts the existing noise sources in this VCO. Using the Thevenin equivalent circuit, the equivalent power spectral density of the two pMOS and nMOS cross-coupled blocks is [Haji 02]

$$\overline{i^2_{w_{eq},d}} = \frac{1}{2}\left(\overline{i^2_{w,d,n}} + \overline{i^2_{w,d,p}}\right) \tag{3.19}$$

In this work the noise coming from the bias circuit is discarded, since we consider we can design this block with a negligible noise characteristics.

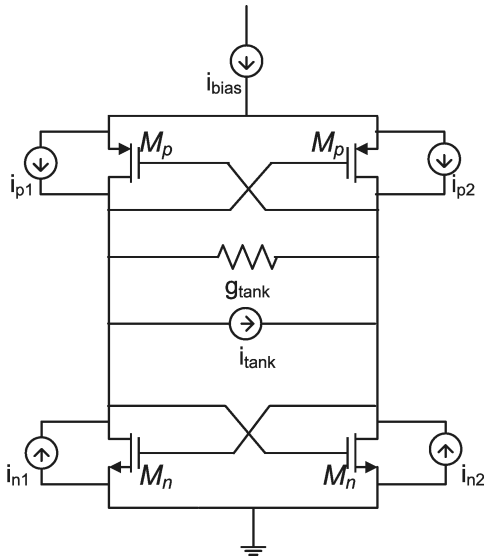


Figure 3.5: *Noise sources in a differential cross-coupled LC-VCO.*

- $1/f^2$ **phase noise expressions**

Substituting the MOS transistor white noise power spectral density of (2.20) into (3.19)

$$\overline{i^2_{w,d,eq}} \cong 4k_BTg_m\frac{1}{2}\Big(\frac{\gamma}{\alpha_n}+\frac{\gamma}{\alpha_p}\Big) = 4k_BTg_m\frac{\gamma}{\alpha_{eq}}. \tag{3.20}$$

with α_{eq} equal to

$$\alpha_{eq} = 2(\alpha_n^{-1}+\alpha_p^{-1})^{-1} = 2g_m\Big(\frac{1}{g_{d0,n}+g_{d0,p}}\Big). \tag{3.21}$$

The white noise of each cross-coupled transistor block due to its equivalent drain-source conductance is [Tsiv 00][BSIM 08]:

$$\overline{i^2_{w,g_{ds}}} = 4k_BT\frac{g_{ds}}{2} = 4k_BT\frac{g_m}{2A_i}. \tag{3.22}$$

The nMOS and pMOS equivalent conductances have jointly the following psd

$$\overline{i^2_{w,g_{ds,eq}}} = 4k_BT\frac{g_m}{2}\Big(\frac{1}{A_{i,n}}+\frac{1}{A_{i,p}}\Big). \tag{3.23}$$

The white noise of the inductor parasitic parallel conductance g_{ind} is

$$\overline{i^2_{w,L_{ind}}} = 4k_BTg_{ind}. \tag{3.24}$$

If g_{var} is comparable to g_{ind}, the white noise power spectral density of the varactor is considered

$$\overline{i^2_{w,C_{var}}} = 4k_BTg_{var}, \tag{3.25}$$

hence, from (3.10), (3.24) and (3.25), the white noise power spectral density of the inductor and the varactor is

$$\overline{i^2_{w,L_{ind}}} + \overline{i^2_{w,C_{var}}} = 4k_BT\frac{g_m}{k'_{osc}} \tag{3.26}$$

Considering that the noise of the MOS conductances, the inductor and the varactor are not correlated, the result of summing the noise given in (3.23) and (3.26) is the tank white noise psd, $\overline{i^2_{w,tank}}$ which is the noise source sketched in Fig. 3.5. Summing the noise of the tank and of the transistors -(3.20), (3.23) and (3.26)-, and using the result of (3.11), the equivalent white noise power spectral density of the VCO is

$$\begin{aligned}
\overline{i^2_{w,VCO}} &= 4k_BTg_m\left(\frac{\gamma}{\alpha_{eq}}+\frac{1}{k'_{osc}}+\frac{1}{2A_{i,n}}+\frac{1}{2A_{i,p}}\right)\\
&= 4k_BTg_m\left(\frac{\gamma}{\alpha_{eq}}+\frac{1}{k_{osc}}\right)\\
&= 4k_BTg_m\xi.
\end{aligned} \tag{3.27}$$

where ξ is

$$\xi = \frac{\gamma}{\alpha_{eq}} + \frac{1}{k_{osc}}. \tag{3.28}$$

Besides, the maximum tank capacitance charge is

$$q_{max} = C_{tank} A_{out}. \tag{3.29}$$

By (3.1)

$$C_{tank} = \frac{1}{4\pi^2 f_0^2 L_{ind}} = \frac{Q_{tank} g_{tank}}{2\pi f_0} \tag{3.30}$$

where the definition of the tank quality factor (energy-based) is used

$$Q_{tank} = \frac{\omega_0 E_{store}}{P_{diss}} = \frac{\omega_0 C_t}{g_{tank}} = \frac{1}{\omega_0 L_{ind} g_{tank}}. \tag{3.31}$$

Substituting (3.13) and (3.30) into (3.29), results

$$q_{max} = \frac{8}{\pi} \frac{I_D Q_{tank}}{(2\pi f_0)}. \tag{3.32}$$

Finally, substituting (3.27) and (3.32) into (3.17), we obtain

$$\mathcal{L}_{1/f^2}(\Delta f) = 10\ log\left(k_B T \frac{\pi^2}{32} \xi \frac{1}{Q_{tank}^2} \Gamma_{rms}^2 \frac{g_m}{I_D} \frac{1}{I_D} \frac{f_0^2}{\Delta f^2} \right). \tag{3.33}$$

3.2.4 $1/f^3$ region phase noise

In this section we develop the model that describes the phase noise in the $1/f^3$ spectrum region for all-inversion regions, starting from (3.18) of the Hajimiri's model [Lee 00]. For the differential cross-coupled LC-VCO, and supposing that only the MOS transistors injects flicker noise, the total power spectral density of the flicker noise sources is (see Fig. 3.5)

$$\overline{i_{1/f}^2} = \frac{1}{2} \left(\overline{i_{1/f,n}^2} + \overline{i_{1/f,p}^2} \right) \tag{3.34}$$

Substituting the flicker noise power spectral density of nMOS and pMOS transistors in (3.34), we have

$$\overline{i_{1/f}^2} = \frac{1}{2} \left(\frac{K_{F,n}\, g_m^2}{C'_{ox} W_n L} + \frac{K_{F,p}\, g_m^2}{C'_{ox} W_p L} \right) \frac{1}{f} \tag{3.35}$$

Substituting (3.32) and (3.35) into (3.18) and reordering the terms to make appear the g_m/I_D ratio, we obtain the following expression for phase noise in the $1/f^3$ zone valid for all inversion regions (when $g_{m,n} = g_{m,p}$)

$$\mathcal{L}_{1/f^3}(\Delta f) = 10\ log\left(\Gamma_{av}^2 \frac{\pi^2}{16^2} \frac{1}{C'_{ox}} \frac{1}{L} \left(\frac{K_{F,n}}{W_n} + \frac{K_{F,p}}{W_p} \right) \frac{1}{Q_{tank}^2} \left(\frac{g_m}{I_D} \right)^2 \frac{f_0^2}{\Delta f^3} \right) \tag{3.36}$$

3.2.5 Phase noise flicker corner frequency as function of g_m/I_D

The LC-VCO flicker corner frequency $f_{c,1/f^3}$ is the frequency where the phase noise asymptotes due to the white noise and the flicker noise intersect. The flicker corner frequency can be written as function of the MOST corner frequency f_c, which is the frequency where the MOS transistor white noise and the MOS transistor flicker noise power spectral densities asymptotically cross.

The flicker noise psd expression of the MOS transistor can be expressed as function of the white noise psd of the MOS transistor and of the transistor corner frequency f_c as

$$\overline{i^2_{1/f,d}} = \overline{i^2_{w,d}} \frac{f_c}{\Delta f} \tag{3.37}$$

with Δf the offset frequency and $\Delta f < f_c$. The corner frequency of a MOST f_c is obtained making equal the expressions of white noise and flicker noise power spectral densities (2.20) and (2.21), resulting in

$$f_c = \frac{K_F}{4k_B T C'_{ox}} \frac{\alpha}{\gamma} \frac{g_m}{I_D} \frac{I_D}{W/L} \frac{1}{L^2} = \frac{K_F}{4k_B T C'_{ox}} \frac{\alpha}{\gamma} \frac{g_m}{I_D} i \frac{1}{L^2} \tag{3.38}$$

namely, it is a function of the MOS transistor inversion level because of the one-to-one relation assumed between g_m/I_D and i (see Section 2.2.1).

To compute $f_{c,1/f^3}$, (3.17) and (3.18) are made equal. $\overline{i^2_w}$ is equal to the equivalent white noise psd of the VCO, $\overline{i^2_{w_{eq}}}$ (see (3.19)), and $\overline{i^2_{1/f^2}}$ is the equivalent flicker noise psd of the VCO or $\overline{i^2_{1/f^2,eq}}$. Also it is defined $f_{c,eq}$ as the equivalent corner frequency of both nMOS and pMOS cross coupled blocks. Finally Δf is evaluated at $f_{c,1/f^3}$. The result is

$$f_{c,1/f^3} = f_{c,eq} \left(\frac{\Gamma_{avr}}{\Gamma_{rms}} \right)^2 = k_o f_{c,eq} \tag{3.39}$$

We find the equivalent corner frequency $f_{c,eq}$ of the MOS transistor by obtained equaling (3.19) to (3.37) and evaluating Δf in the corner frequency $f_{c,eq}$, as follows

$$\overline{i^2_{w,eq}} = \frac{1}{2}\left(\overline{i^2_{w,n}} + \overline{i^2_{w,p}}\right) = \frac{1}{2}\left(\overline{i^2_{1/f,n}} + \overline{i^2_{1/f,p}}\right)|_{f_{c,eq}} = \frac{1}{2}\left(\overline{i^2_{w,n}} \frac{f_{c,n}}{f_{c,eq}} + \overline{i^2_{w,p}} \frac{f_{c,p}}{f_{c,eq}}\right) \tag{3.40}$$

Solving, we have

$$f_{c,eq} = \frac{\overline{i^2_{w,n}}\, f_{c,n} + \overline{i^2_{w,p}}\, f_{c,p}}{\overline{i^2_{w,n}} + \overline{i^2_{w,p}}}. \tag{3.41}$$

This result is valid both for the simplified approach studied in this section and for the general model considered in Section 3.3.

3.2.6 Comments about the phase noise model

To estimate the Γ_{av} and Γ_{rms} data, we use the method presented for Hajimiri (Appendix C of [Haji 98]), $\Gamma = f'(x)/f'^{2}_{max}$, where f' represents the derivative of the normalized waveform at the VCO output, f'_{max} is its maximum and x the phase in radians. Being the normalized waveform at the output $V_{out}(x)$, $\Gamma(x)=V_{out}(x)'/V'^{2}_{out_{max}}$. We obtain V_{out} by simulation, and $\Gamma(x)$ with the previous equation. Then by applying the FFT to $\Gamma(x)$ we obtain its spectal contents $\{c_n\}$.

We have used this procedure in a MATLAB routine that emulates the signal and distortion behavior of the desired VCO. For our specifications, $\Gamma_{rms} = 0.5$, $\Gamma_{av} \leq 0.4$ and $k_0 \leq 0.16$. It means that $f_{c,1/f^3}$ is generally much smaller than f_c. Γ_{av} is dramatically reduced if the output signal is a low distorted sinusoidal waveform.

The $1/f^2$ and $1/f^3$ phase noise expressions we provide here help the designer to quantitatively visualize the compromises between phase noise and current consumption. Considering a fixed g_m, imposed by the oscillation condition (3.12), when g_m/I_D rises, i.e when moving towards weak inversion, I_D decreases in the same proportion. Rising g_m/I_D and reducing I_D leads to a phase noise increment in the $1/f^2$ and $1/f^3$ spectrum regions. The design methodology flow, developed next, explores these trade-offs, making it possible to optimize consumption while achieving the specified phase noise level.

3.2.7 Design methodology flow

Arriving at this stage of the process, the designer has the analytical expressions which describe the VCO under study. From Chapter 2, the components database is also familiar. Therefore, it is all ready to do the final step of the general methodology: the development of a VCO design flow.

- **Differential LC-VCO design flow**

To accomplish the VCO design flow, the design constraints and specifications of the LC-VCO should be known in advance. The constraints considered in this study are:

1. the maximum power consumption, which is translated into a maximum acceptable quiescent drain current, $I_{D,max}$, flowing through the pMOST and nMOST.

2. the minimum signal output voltage $A_{out,min}$ which makes possible the correct operation of the stage that follows the VCO.

3. the minimum varactor capacitance $C_{var,min}$ that makes a feasible varactor and assures that the variations in the fabrication parameters do not significantly affect the VCO features.

4. the maximum flicker corner frequency, $f_{c,1/f^3}$; below that frequency, the phase noise model that should be used is the one that corresponds to the flicker zone, $\mathcal{L}_{1/f^3}$.

5. the maximum acceptable phase noise $\mathcal{L}_{1/f^2,max}$ at a frequency offset Δf.

Initially the hypothesis that the offset frequency Δf is above $f_{c,1/f^3}$ is assumed, so the expression of the phase noise used is the one of (3.33). If it is not the case that design is discarded. To add a level of complexity to the flow we could remove this constraint and use the $1/f^3$ phase noise expressions together with the $1/f^2$ phase noise expressions to do the computations. For close-in phase noise VCOs [Isma 03], where the $1/f^3$ region is fundamental for this phase noise calculations, the referred initial hypothesis does not apply.

The flow diagram is sketched in Fig. 3.6, and it is organized in the following steps:

Step 1) Start fixing a set of initial parameters and limits: minimum transistor channel length L_{min}, safety margin factor k_{osc}, maximum equivalent inductance $L_{ind,max}$, minimum varactor capacitance $C_{var,min}$ and C_{load}. Next, set the VCO specifications: oscillation frequency f_0, maximum current $I_{D,max}$, maximum phase noise in the white noise zone $\mathcal{L}_{1/f^2,max}$ at an offset Δf and minimum output voltage $A_{out,min}$.

Step 2) Pick a pair of values of inductor L_{ind} and g_m/I_D ratio (equal for nMOS and pMOS transistors), from the technological LUTs of inductors ($\Lambda_L^{(p)}$) and transistors, which is assumed previously collected, as it was shown in Chapter 2.

Step 3) From the inductors database $\Lambda_L^{(p)}$, derive the g_{ind} of that inductor. Obtain the normalized currents of nMOS and pMOS, i_n and i_p, as well as $g_{ds}/I_D = (g_{ds}/I_D)_n = (g_{ds}/I_D)_p$, from the picked g_m/I_D and the characteristic curves g_m/I_D vs. i and g_{ds}/I_D vs. g_m/I_D. Calculate the intrinsic gains $A_{i,n}$ and $A_{i,p}$ from (3.8) and then deduce k'_{osc} using (3.11). Extract the transistors equivalent capacitance from $C'_{ij,n}$ and $C'_{ij,p}$ versus g_m/I_D LUTs.

Step 4) Deduce g_m from (3.12). With g_m and g_m/I_D calculate the drain current I_D, and with (3.13) compute A_{out}. Then, calculate the transistors widths W_n and W_p from I_D and i_n and i_p and compute $C_{ij,n}$ and $C_{ij,p}$. With (3.1), (3.4) and (3.6), solve for C_{var}. Calculate $f_{c,1/f^3}$ using (3.39).

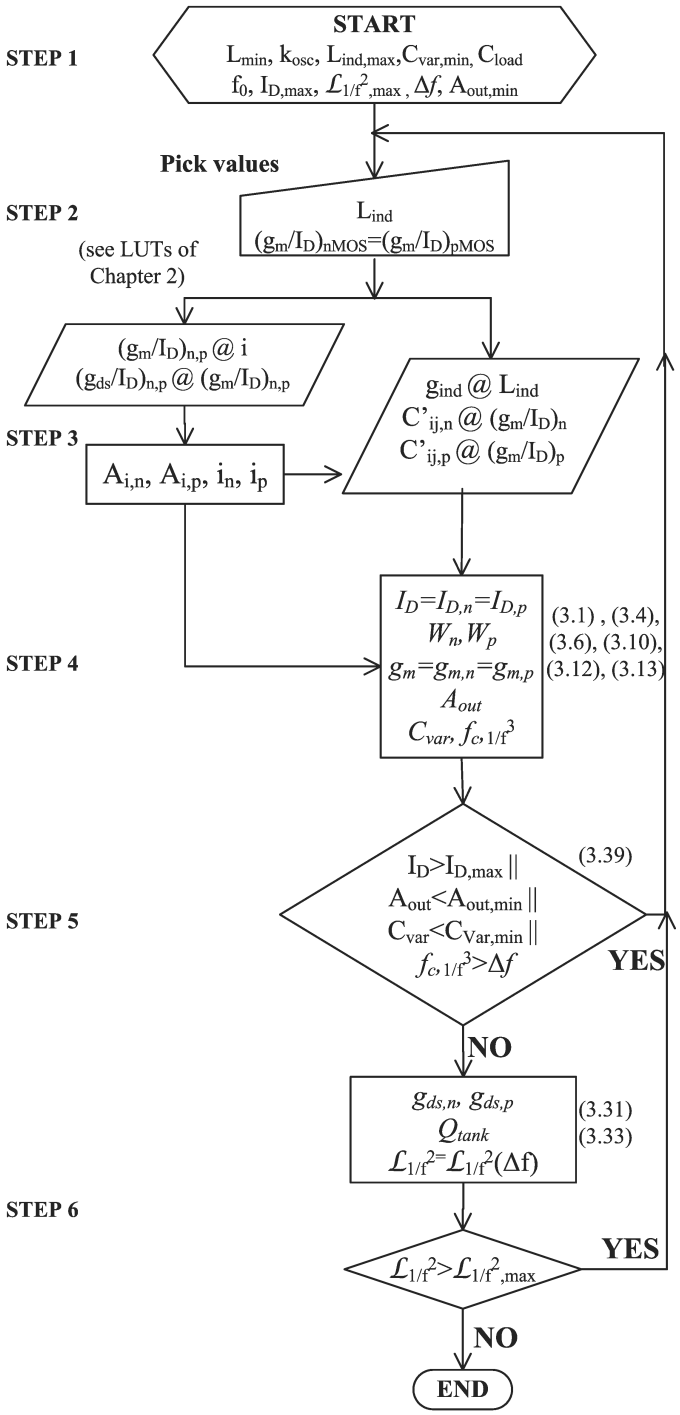


Figure 3.6: *Flow diagram for the differential LC-VCO design.*

Step 5) If $I_D > I_{D,max}$ or $A_{out} < A_{out,min}$ or $C_{var} < C_{var,min}$ or $f_{c,1/f^3} > \Delta f$, return to ***Step 2*** and change one or both of the values chosen, otherwise continue.

Step 6) Compute $g_{ds,n}$ and $g_{ds,p}$ and hence, Q_{tank} with (3.31). Calculate the phase noise $\mathcal{L}_{1/f^2}$ using (3.33) at the frequency offset Δf. If it surpasses $\mathcal{L}_{1/f^2,max}$, return to ***Step 2***, otherwise the design is finished.

- **Contour maps**

This section presents a set of MATLAB design maps obtained with the design flow under the simple approach hypothesis, in order to see the efficacy and the potential of the method.

We implemented the design flow in a set of computational routines to graphically study the behavior of the phase noise, the current consumption and the flicker corner frequency when g_m/I_D and L_{ind} change. The initial parameters were: f_0=2.4 GHz, k_{osc}=3 and C_{load}=250 fF. As TECH2 data have been utilized throughout the routines, for more insight, some technology curves, as g_m/I_D versus i or the maximum parallel resistance available for each feasible inductance are presented in Appendix 2.C.

Initially, the relation between I_D and g_m/I_D is studied in Fig. 3.7, for four inductor values. A decrement in I_D can be appreciated when: (a) g_m/I_D rises (i.e. when moving towards weak inversion), and (b) if the inductance value increases. The point (a) is explained because g_{ind} is fixed for each L_{ind} so, from (3.12), g_m is fixed. Thus, when g_m/I_D increases, necessarily I_D decreases. The point (b) is deduced from Fig. 2.25, where an increment in the inductor value means an increment in its parallel resistance. This implies a reduction in g_{ind}, and thus in g_m, due to (3.12).

Another interesting characteristic is the $1/f^2$ phase noise versus g_m/I_D, con-

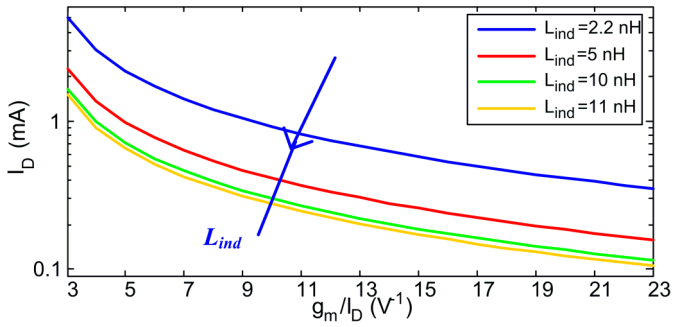


Figure 3.7: *Drain current I_D versus g_m/I_D for four inductance values L_{ind} for the differential LC-VCO simplified model.*

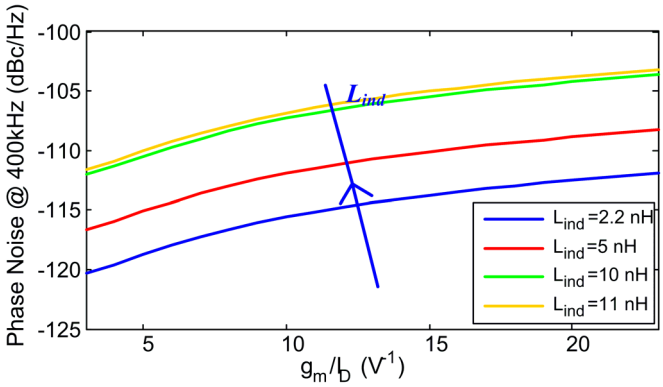


Figure 3.8: *Phase noise in the $1/f^2$ region versus g_m/I_D for four inductance values L_{ind} for the differential LC-VCO simplified model.*

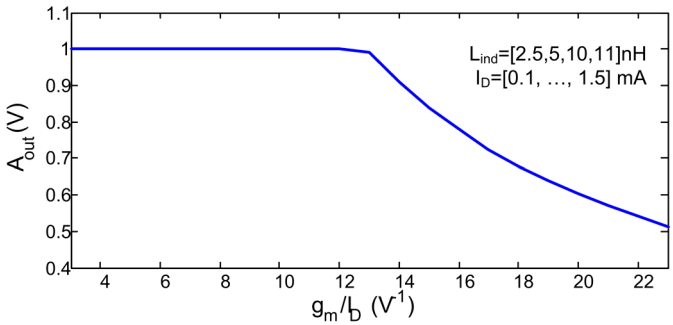


Figure 3.9: *A_{out} versus g_m/I_D for the differential LC-VCO simplified model.*

sidering again four inductor values, visualized in Fig. 3.8. Phase noise increases when working in moderate and weak inversion because it is proportional to g_m/I_D, as (3.33) states. It also increases for low inductor values, because these inductors have higher g_{ind}, which, due to (3.31), cause low tank quality factors Q_{tank}; being Q_{tank} inversely proportional to $\mathcal{L}_{1/f^2}$.

Likewise, the signal output voltage amplitude A_{out} changes with the g_m/I_D ratio, as depicted in Fig. 3.9. It is independent of the I_D current or the tank inductor L_{ind}, as (3.13) stands. As expected, A_{out} decreases when moving through weak inversion because it is inversely proportional to g_m/I_D. The maximum differential output voltage of the tank is limited due to the supply and the current source and this effect is shown with the constant line of the graph; which in this case $A_{out,max}$ is 1 V and occurs for g_m/I_D ratios below 13 V^{-1}.

Varactor capacitance also changes with the inversion region and obviously, with the inductance value. In Fig. 3.10 we can appreciate a reduction in C_{var} when moving through moderate and weak inversion. This behavior is expected as in MI

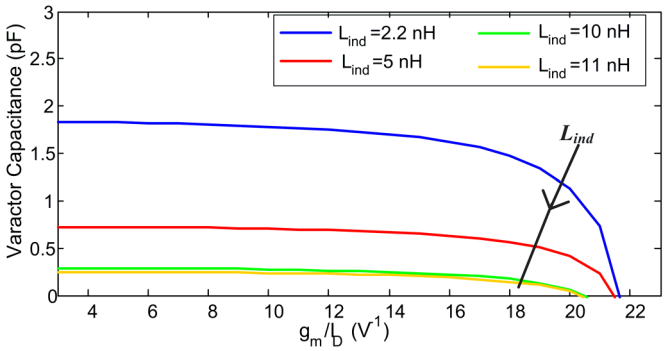


Figure 3.10: *Varactor capacitance versus g_m/I_D for four inductor values considering differential LC-VCO simplified model.*

and WI the transistor increases its size and hence, its parasitic capacitances, leaving less room for the varactor capacitance value. It also decreases with an inductor increment, as expected from expression (3.1). From Fig. 3.10 it is observed that after a given g_m/I_D value, C_{var} would be low enough not to reach the minimum acceptable $C_{var,min}$, and as a consequence the g_m/I_D values above that value are discarded .

The behavior of the MOS transistor corner frequency $f_{c,eq}$ and the VCO flicker corner frequency $f_{c,1/f^3}$ as functions of g_m/I_D are presented in Fig. 3.11, using (3.38) and (3.39). The constant values used are $\Gamma_{av} = 0.2$ (as a sinusoidal V_{out} is considered), and the values of TECH2 K_F, $K_{F,n} = 5 \cdot 10^{-25} JHz$ and $K_{F,p} = 20 \cdot 10^{-25} JHz$. An interesting observation is the fact that MOS transistor corner frequency decreases when moving towards weak inversion, and the VCO flicker corner frequency also decreases in weak inversion. The reduction of $f_{c,1/f^3}$ is a good consequence of working in weak and moderate inversion regions as the phase noise is lower in the $1/f^2$ region, as has been already stated.

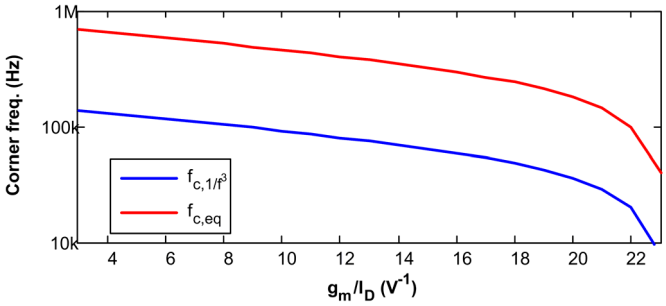


Figure 3.11: *Corner frequencies $f_{c,eq}$ and $f_{c,1/f^3}$ for the differential LC-VCO simplified model.*

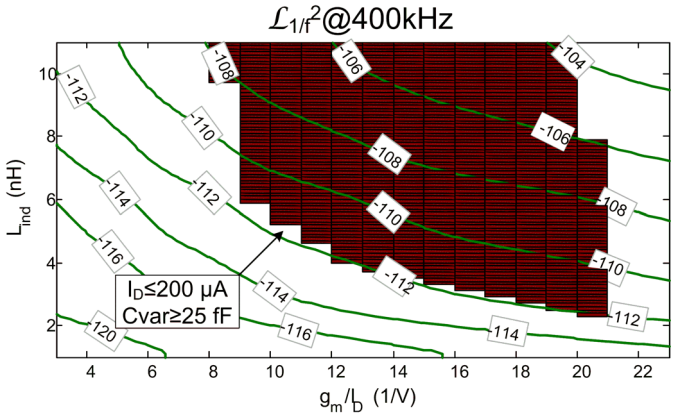


Figure 3.12: *$\mathcal{L}_{1/f^2}$ in dBc/Hz mapped versus g_m/I_D and L_{ind}.*

Finally, we generate the design map of Fig. 3.12. It presents the phase noise behavior when jointly vary g_m/I_D and L_{ind}. We add a shadowed zone to exemplify a boundary inside which the current is below the specification limit of $I_{D,max}$=200 μA jointly with varactor capacitance above the specification of $C_{var,min}$=25 fF, a shadowed zone is added. For the chosen example, it is clear that for g_m/I_D above 21, which means high transistor widths, there is an invalid zone, because varactor capacitances are very small or even negative. For g_m/I_D below 8, the current surpasses the 200 μA and, again, it is an invalid zone. g_{ind} increases for very low inductors and due to the condition of oscillation, thus also g_m does. It is translated to high bias currents, and that is why does not exist a valid design for inductors below 2.5 nH. Studying the phase noise behavior, the abovementioned observations arise again: for high inductors the phase noise is higher than for low inductors, as the tank quality factor is smaller for high inductors. Finally, for weak inversion the phase noise is higher than for strong inversion, as expected from the expressions (3.33).

Figures 3.7 to 3.12 show the potential of our methodology, as these plots easily highlight the trade-offs of the VCO characteristics in the different MOST inversion regions.

3.2.8 Validation by simulation

We present in this section four 2.4-GHz LC-VCO examples designed in the TECH2 with the simplified modeling, obtained from the design methodology flow of Section 3.2.7. These examples are compared to highlight the trade-offs in different design zones. This study reasserts the general ideas discussed in Chapter 1, showing the utility of the method and the compromises between the three operation re-

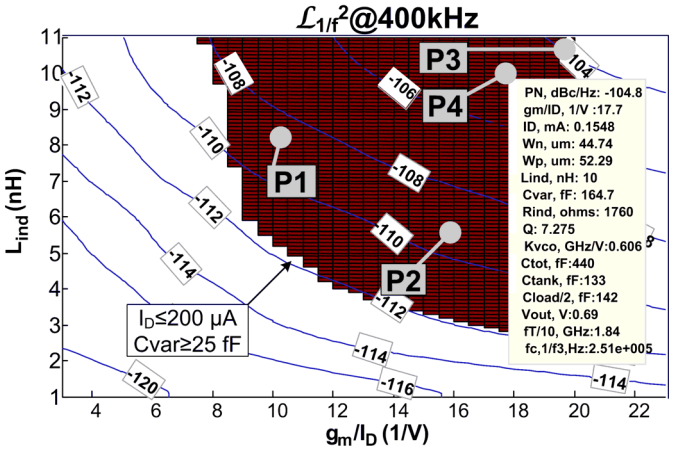


Figure 3.13: *$\mathcal{L}_{1/f^2}$ in dBc/Hz mapped versus g_m/I_D and L_{ind}. The text-box displays the characteristics and parameters of the LC-VCO associated with the picked point (P4 in this example).*

gions. Moreover, to validate the results obtained in the comparison, we contrast the characteristics of these examples with their respective SpectreRF simulations. This way, it is checked the similarity of the computation and electrical full simulation data. To perform a general validation of the all-inversion region VCO methodology, each example belongs to a different zone of the design map, namely WI, MI and SI, and high or low inductors.

The data of the four examples are picked from the computational routines and showed in Fig. 3.13, where they are referred as *P1*, *P2*, *P3* and *P4*. The constraints

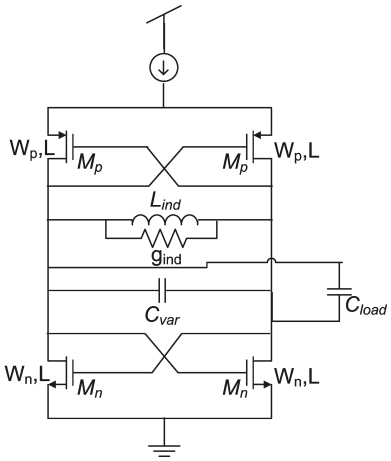


Figure 3.14: *Schematic used in SpectreRF to check the design points P1 to P4.*

of drain current $I_{D,max} \leq 200\mu A$ and varactor capacitance $C_{var,min} \geq 25\ fF$ are set and limit the possible designs to the shadowed area of the plot. Also, the phase noise of these design points is limited to $\mathcal{L}$ <-100 dBc/Hz at 400 kHz. For the computations, $\Gamma_{av} = 0.2$ and $k_0 = 0.04$, as the V_{out} is supposed very sinusoidal. The schematic shown in Fig. 3.14 has been used.

The design points are distributed in the design map as follows: *P1* is in the limits of strong inversion, *P3* is in the limits of weak inversion and, *P2* and *P4* are in moderate inversion. Considering the position respect to the inductor values, *P3* and *P4* use high inductors, and *P1* and *P2* utilize inductors in the midst of the range. Table 3.1 compares the VCO data obtained with the simple approach design flow formulas and with the data derived with SpectreRF analysis. The quasi-static limit considered is the one of the pMOS transistor, as it has lower values of f_T, as shown in Fig. 2.7 of Chapter 2. Considering the "Computed" column of Table 3.1 we observe that although design points *P1* and *P2* are very similar in terms of phase noise (-107.3 dBc/Hz versus -109.4 dBc/Hz), *P1* consumes 215 μA and *P2* 315 μA, a 46% more, and *P1* has also a higher inductor. These advantages are opposed to the fact that *P2* will work below the quasistatic-limit frequency ($f_T/10 = 3\ GHz$) whereas *P1* is far below it ($f_T/10 = 8.6\ GHz$). Analyzing designs *P3* and *P4*, we observe that the first one consumes 16% less (130 μA respect to 155 μA) and has a phase noise only 0.8 dB higher than the second one (-104 dBc/Hz and -104.8 dBc/Hz, respectively). However *P4* is nearer the quasi-static limit than *P3* ($f_T/10_{P3} = 1.1\ GHz$ versus $f_T/10_{P4} = 1.7\ GHz$), therefore it is not recommendable to choose *P3* when the working frequency is $f_0 = 2.4$ GHz.

Let us now perform the comparison between the "Computed" and the "SpectreRF" results of each design point of Table 3.1. The Computed and the SpectreRF results of designs *P2*, *P3* and *P4* in terms of signal output voltage, phase noise, quasistatic-limit frequency or corner frequency have slight -and expected- differences. The point *P1* only differs in the phase noise results as $\mathcal{L}_{computed} = -107.3\ dBc/Hz$ whereas the $\mathcal{L}_{SpectreRF} = -110\ dBc/Hz$. We consider that the cause of this difference is that the noise constants are fixed to one particular value in all the design map, whereas as we have seen in Chapter 2 these values change; and obviously this fact is reflected in the SpectreRF model (PSP model, in TECH2).

The flicker corner frequency lines of Table 3.1 show the predicted fact that working in strong inversion increases the flicker corner frequency. It is also appreciated in Fig. 3.15 which shows the phase noise of the four designs versus the frequency offset Δf, obtained from SpectreRF simulations. For low offset frequencies, the phase noise curve of *P1* has a higher slope that the ones of the *P2*, *P3* and *P4*. It means that the flicker noise begins to have an influence in this zone, and for lower g_m/I_D this effect is sharper.

From the presented designs, the computed results of the quasistatic-limit frequency state that strictly, only *P1* and *P2* should be used for a working frequency of

Table 3.1: *Characteristics of the chosen designs in SI, MI and WI for f_0=2.4 GHz*

Parameter	*P1* (SI)		*P2* (MI)		*P3* (WI)		*P4* (MI)	
	Computed	SpectreRF	Computed	SpectreRF	Computed	SpectreRF	Computed	SpectreRF	Fabricated
I_D (μA)	315	315	215	215	130	130	155	155	165
W_n (μm)	8.8	8.8	37	37	76.2	76.2	45	45	10×4.6
W_p (μm)	23.6	23.6	50.1	50.1	78.6	78.6	53	53	10×5.4
L_{ind} (nH)	8	8	5.5	5.5	10.7	10.7	10.1	10.1	10
C_{var} (fF)	255	255	537	537	60.3	60.3	165	165	175
g_m/I_D (V^{-1})	11.2	9.9	16.1	14.5	19.6	19.3	17.7	17.4	17.6
A_{out} (V)	1.3	1.3	0.77	0.96	0.62	0.74	0.7	0.87	0.8
$\mathcal{L}$ (dBc/Hz@400kHz)	-107.3	-110	-109.4	-110.2	-104	-103.2	-104.8	-104.6	-104.3
$f_T/10$ (GHz)	8.6	8.7	3	1.9	1.1	0.9	1.7	2	1.8
$f_{c,1/f^3}$ (kHz)	179	210	87.3	58	38.2	65	63.2	67	72

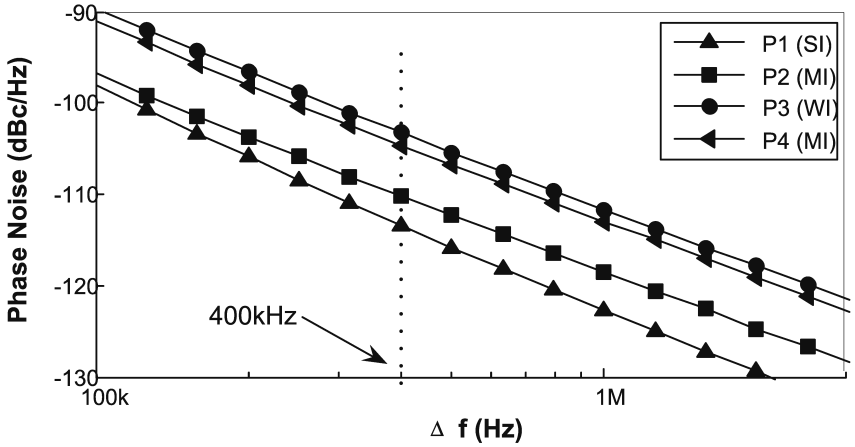


Figure 3.15: *Electrically simulated phase noise for the four design points of Fig. 3.12.*

2.4 GHz. However, we can relax a bit this limit due to the fact that PSP models the channel in a continuous manner from a quasistatic state to a non-quasistatic one. We can go up to a third of f_T if the transcapacitances are included (see [Tsiv 00]), however, the presented methodology does not consider them.

It is important to mention that the fingers of all the transistor widths were adjusted in the schematic in order to make negligible the gate resistance, as it has not been considered as a variable in the design flow.

Finally, from the four designs, *P4* is chosen to validate experimentally the methodology. This point allows us to play with the bias current, to visualize its effect in the phase noise and to experimentally check the relationships discussed above. Final VCO component sizes and simulated characteristics are listed in the last column of Table 3.1. As the output of the fabricated VCO has an on-chip differential-pair buffer to fix C_{load}, minor components resizing were needed to tune the desired oscillation condition, oscillation frequency and phase noise.

3.2.9 Experimental validation

The design kit of TECH2 does not provide I/O pads for radio-frequency, supply voltage or ground signals, but it has a robust ESD library, so we design our own pads with ESD protection. An output VCO buffer has been designed to fix the load capacitance of the VCO as it will be explained next with more detail. The characteristics of the VCO are measured on bare die using a microprobe station; the RF pads are spaced out 100 μm in order to land the RF probes. The die is sticked to a LCC28 package and only the DC voltages are soldered to its pins through bondwires.

The schematic of the fabricated VCO using the data of P4 of Table 3.1 is depicted in Fig. 3.16 and its layout in Fig. 3.17. The total chip is shown in Fig. 3.17.(a), with the voltages and currents of the VCO VDDVCO, IbiasVCO, Vcontrol; the current of the buffer IbiasBuff; the bias of the pad ring VDDRING and the general ground GND. The output signals are V0BUFF+ and V0BUFF-. The final VCO design occupies an area of 500 $\mu m \times 350\ \mu m$ as Fig. 3.17.(b) shows. The microphotograph of the chip is shown in Fig. 3.17.(c).

- **Output Buffer**

In order to fix the output load of the designed VCO, a common-source differential pair with on-chip load has been used. Its scheme is presented in Fig. 3.18. The current I_{buff} biases the transistors M_{buff} and the resistances R are used to fix the gain of the group. It is desired that the total gain of each branch, equal to $g_m R$, will be the unity, in order to have the same signal value at the output of the buffer than at the output of the LC-VCO. The capacitors C_{dec} are included inside the chip to decouple the DC signal of the transistor biasing from the RF output signal with the 50 Ω load of each branch. The transistors are biased in very strong inversion in order to cope with the high signal output voltages of the VCO without distorting that signal.

To adjust the differential pair gain to 1, the I_{buff} is fixed to 18 mA and the transistor W/L is 202 $\mu m/200\ nm$, generating a transconductance $g_{m,buff} = 0.0192$ S,

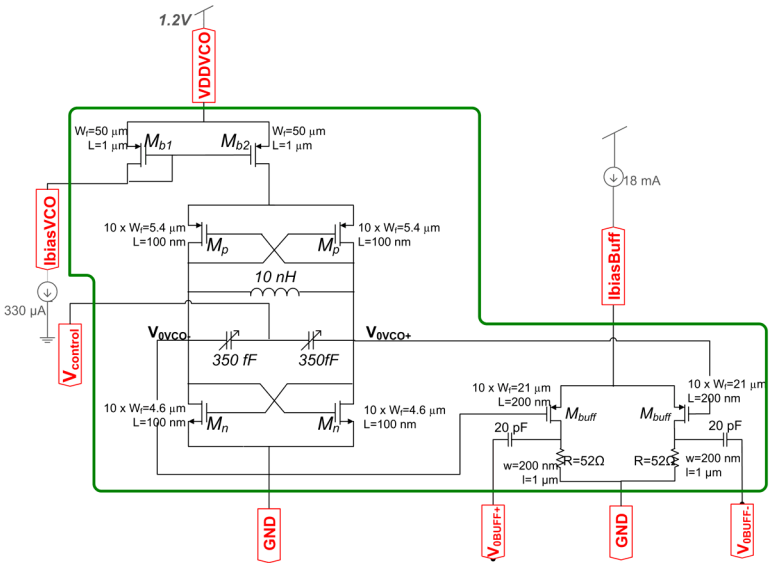


Figure 3.16: *Schematic of the fabricated VCO*

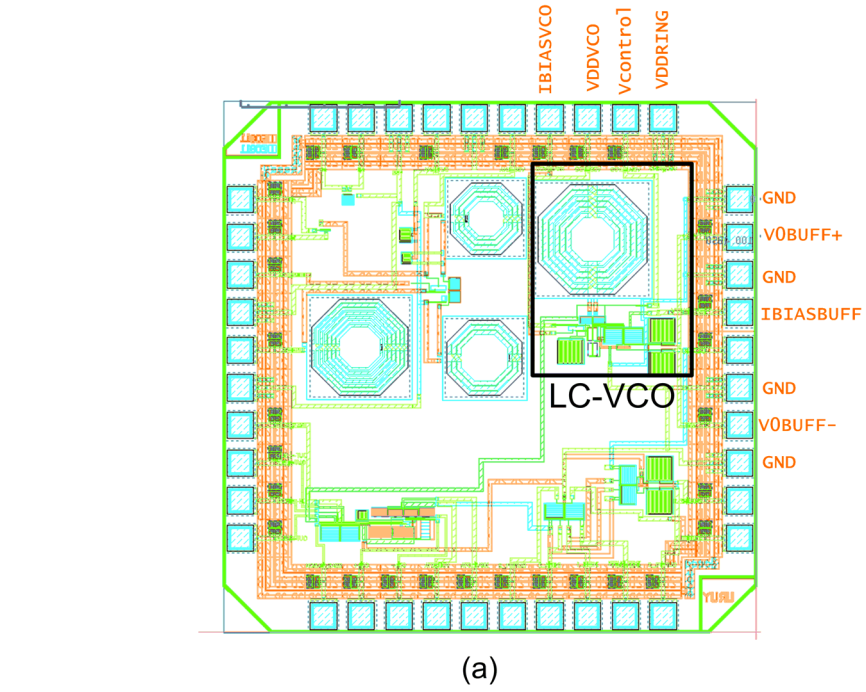


Figure 3.17: *(a) Layout of the total chip; (b) zoom of the designed LC-VCO and (c) microphotograph of the fabricated chip.*

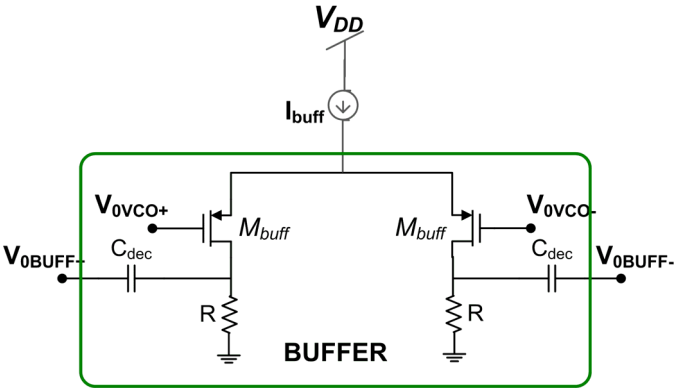


Figure 3.18: *Schematic of buffer used at the output of the LC-VCO*

inversely proportional to the resistance R equal to 52 Ω. The g_m/I_D of the pair is around 2.1, which, from tables, represents a normalized current i=40 μA. Utilizing the expression of the linearity of [Arna 03]

$$V_{lin} = 2nU_T \sqrt{\frac{6\alpha_{lin}(1+i_f)^{3/2}}{3(1+i_f)^{1/2}-1}} \tag{3.42}$$

where V_{lin} is the input linear range defined in terms of the acceptable error α_{lin} (i.e. $\alpha_{lin} = 5\%$), the slope factor n, the thermal voltage U_T and i_f defined in (2.4) we can check how good is the buffer. It would be desirable to work with a linear range with an error around 5%, then $V_{lin} = 0.95V_{out} \cong 0.76\ V$, with a fabricated $A_{out} = 0.8\ V$ (see Table 3.1). For this design, from (3.42), $V_{lin} = 0.79\ V$, which exceeds the specifications.

- **Differential LC-VCO experimental results**

The characterization has been performed for three samples, the results of the measurements do not vary noticeably among them. The measures done have been: (a) the working frequency f_0 versus the control voltage $V_{control}$, (b) the phase noise spectrum for a certain bias current, and (c) the phase noise at a certain offset for several bias currents. The equipment utilized to characterize the fabricated LC-VCO was: (a) the Agilent Spectrum Analyzer E4440A, employed to characterize its spectrum and phase noise; and (b) the microprobe station, the Cascade Microtech M150, with the set of single-ended microprobes. The experiment set-up is shown in Fig. 3.19.

Unfortunately, the buffer did not work properly and interfered with the VCO behavior, so the phase noise measurements were done with the output buffer switched off in order to stabilize the signal. Only the output signal amplitude measurements

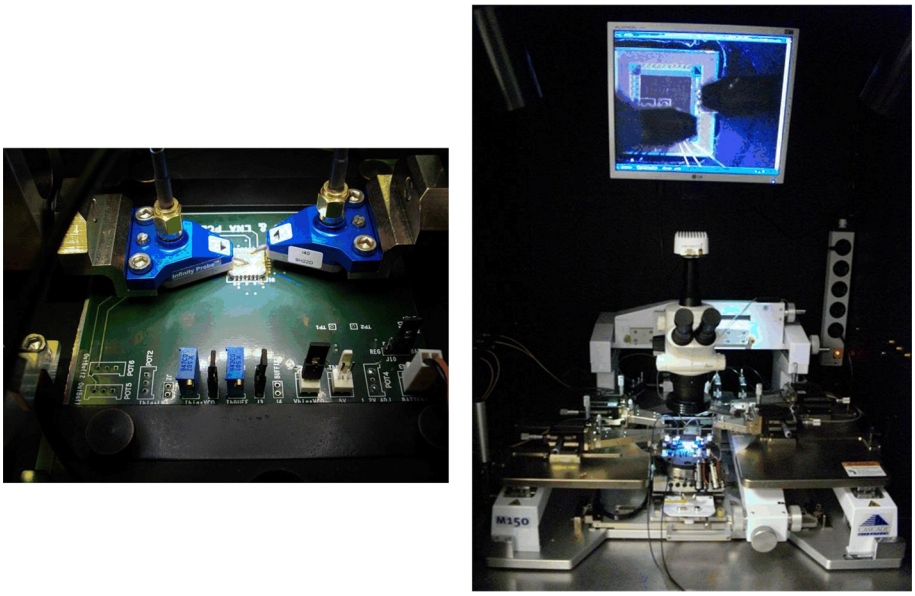


Figure 3.19: *Photographs of the LC-VCO measurement set-up.*

were done with the buffer switched on, only to have a rough value of the maximum output amplitude reachable. Despite the several attempts done trying to find and solve the malfunctioning we were not able to improve the behavior of the buffer.

Figure 3.20 displays the variation of f_0 with control voltage $V_{control}$ when the buffer is switched off. The $V_{control}$ has been swept between 0 V and 1 V and the frequency varied between 2.16 GHz and 2.5 GHz. The VCO gain K_{VCO} is 0.48 GHz/V and it is valid between 0.2 V and 0.7 V approximately. Figure 3.21 shows the VCO spectrum for a $V_{control} = 0V$, measured with the buffer off -which is obvious due

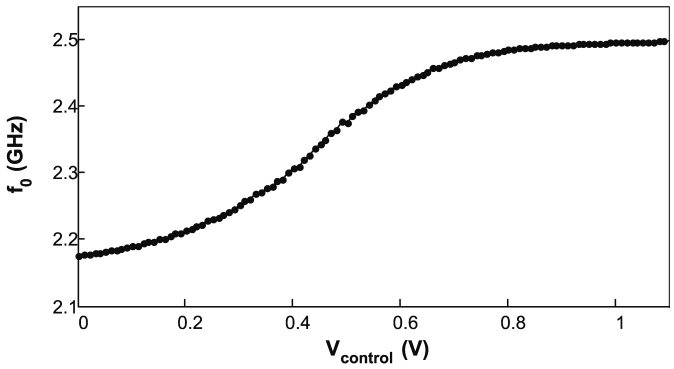


Figure 3.20: *Carrier frequency f_0 versus $V_{control}$ with the buffer switched off.*

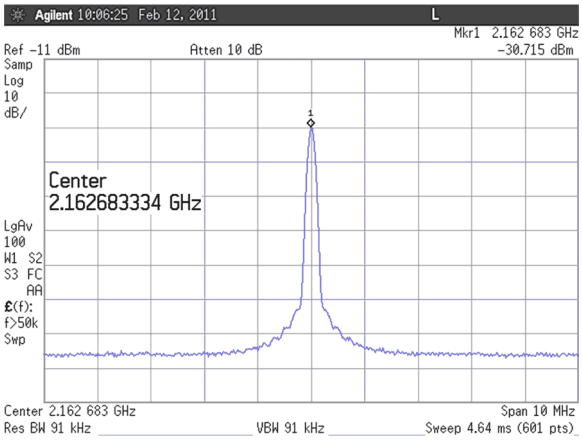


Figure 3.21: *Output spectrum of the VCO with* $V_{control} = 0\,V$.

to the low power output amplitude, around -30dBm-. The minimum bias current where a clean spectrum without interferers was obtained is I_D=220 μA. For this current, the phase noise versus the offset frequency, with the carrier at 2.16 GHz ($V_{control} = 0V$) is shown in Fig. 3.22. The phase noise at 400 kHz from the carrier is -106.2 dBc/Hz. The measured flicker corner frequency $f_{c,1/f^3}$ is 203 kHz, whereas the simulated flicker corner frequency, shown in Table 3.1, is 72 kHz. This rise in $f_{c,1/f^3}$ respect to the simulated data of *P4*, happens because V_{out} is distorted when the buffer is turned off. Γ_{av} rises to approximately 0.4, and the computed $f_{c,1/f^3}$ is 257 kHz, very near the measured data.

The current I_D was also swept to 310 μA and a set of phase noise measurements at 400 kHz from the carrier were performed (forty measurements of $\mathcal{L}$ were taken for each current value), as depicted in Fig. 3.23, considering again a carrier

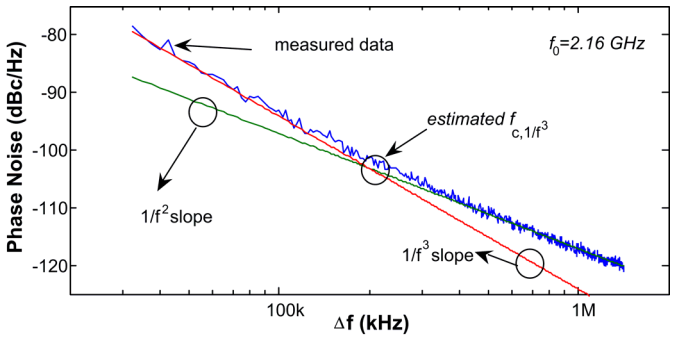


Figure 3.22: *$\mathcal{L}$ with the VCO biased with $I_{bias} = 2 \cdot I_D = 440\mu A$ and $f_0 = 2.1639GHz$ (buffer switched off). $1/f^2$ and $1/f^3$ slopes are shown as well as the estimated flicker corner $f_{c,1/f^3}$.*

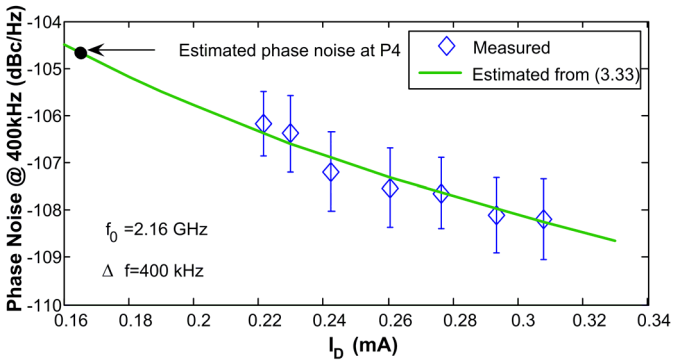


Figure 3.23: *Phase noise measured and estimated by* (3.33)*, sweeping only* I_D.

frequency around 2.16 GHz. The theoretical curve of (3.33) is superimposed with experimental data, considering $\alpha = 0.65$, $k_{osc} = 3$ and $\gamma = 0.55$. The fitted model is extended up to the nominal I_D current of 165 μA, obtaining an extrapolated phase noise value of -104.6 dBc/Hz. Good agreement exists between model, simulations and measurements.

The minimum measured I_D where the VCO worked, for three samples' average, is 62.5 μA; 13.5% higher than the expected value of 52 μA obtained from the design flow. The output voltage when the buffer was switched on to a $I_{buff} = 15\ mA$, for I_{bias}=440 μA is 630 mV, a bit lower than expected. The $I_{biasBuff}$ could not be increased to the nominal value of 18 mA because for higher currents it generated subharmonics peaks around the fundamental frequency and raised the noise floor.

Table 3.2 compares the performance of the designed LC-VCO in moderate inversion with that of some prior works, where the well-known figure-of-merit (FoM) of the VCO defined in [Park 08] is used

$$FoM = 10log\left(\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{\mathcal{L}(\Delta f)P_{DC}}\right) \tag{3.43}$$

Table 3.2: *Performance Comparison of recently published LC-VCOs.*

VCO	Tech. (nm)	f_0 (GHz)	Δf (MHz)	Power (mW)	$\mathcal{L}$ (dBc/Hz)	FoM (dB)
[Leun 08] 2008	180	2.2	1	5.17	-119	179
[Lee 07] 2007	180	2.645	0.4	0.63	-106.4	184.8
[Peru 08] 2007	180	2.5	1	1.2	-103.7	171
[Park 08] 2008	180	1.57	1	3.06	-120	180
This work	90	2.16	0.4	0.53	-106.2	183.6

where P_{DC} is the power consumed by the VCO, while the other parameters were already presented.

Our VCO is well positioned considering other similar designs, as only the second one has a better FoM. However the later occupies more area than our design because it uses two on-chip inductors, which increases the tank quality factor and reduces the phase noise.

3.3 Cross-coupled differential LC-VCO: general approach

The simple approach imposes the restriction of equal transconductances of pMOS and nMOS transistors. It is translated to equal the g_m/I_D ratio of these transistors as the drain current is considered identical for pMOS and nMOS transistors. It means that both transistors follow the same inversion region. When this constraint disappears, both transistors could be in different inversion regions. If the phase noise minimization condition is applied, and if the g_m/I_D ratio of one type of MOS transistor is swept (for example the nMOS), it is found that the other type of MOS transistor (in the example, the pMOS) will pick the lowest g_m/I_D available in order to reduce the phase noise. If it is applied a current minimization condition, the results are the opposite, for a fixed g_m/I_D of one type of MOS transistor, the g_m/I_D ratio of the other type of MOS transistor will increase to the maximum available. These statements will be clear with the new expressions of current and phase noise.

A first consequence of lifting the restriction when the phase noise minimization condition is applied is to have lower phase noise. However, as the current is not fixed, it tends to increase respect of the simple approach current consumption results. When current minimization is applied, the phase noise tends to increase respect to the simple approach. It means that the generic approach could improve the phase noise at the expense of higher consumption or vice versa.

3.3.1 Signal modeling

For this general approach the oscillation condition given in (3.7) is transformed into

$$g_{m,n} + g_{m,p} = 2\ k_{osc} g_{tank} \tag{3.44}$$

Substituting (3.9) into (3.44), the tank conductance changes from (3.10) to

$$g_{var} + g_{ind} = g_{m,n}\left(\frac{1}{2k_{osc}} - \frac{1}{2A_{i,n}}\right) + g_{m,p}\left(\frac{1}{2k_{osc}} - \frac{1}{2A_{i,p}}\right). \tag{3.45}$$

The output voltage amplitude is now

$$A_{out} \cong \frac{8}{\pi}\frac{2k_{osc}}{g_{m,n}/I_D + g_{m,p}/I_D}. \tag{3.46}$$

The current I_D is calculated by applying the expression (3.45), dividing it by I_D and assuming that g_{var} is negligible respect the total tank conductance:

$$2\frac{g_{ind}}{I_D} = (g_m/I_D)_n \frac{1}{k'_{osc,n}} + (g_m/I_D)_p \frac{1}{k'_{osc,p}} \tag{3.47}$$

with $k'_{osc,n(p)}$

$$k'_{osc,n(p)} = (1/k_{osc} - 1/A_{i,n(p)})^{-1} \tag{3.48}$$

Rewriting (3.47)

$$I_D = \frac{2g_{ind}}{(g_m/I_D)_n 1/k'_{osc,n} + (g_m/I_D)_p 1/k'_{osc,p}} \tag{3.49}$$

The expressions of oscillation frequency f_0, (3.1), C_{tank}, (3.4), g_{tank}, (3.5) and C_{MOS}, (3.6), are still valid . The new expressions of phase noise and flicker corner frequency are presented next.

3.3.2 $1/f^2$ region phase noise

The advanced approach hypothesis, which lift the constraints of equal nMOS and pMOS transconductances, changes the equivalent power spectral density of the cross-coupled differential MOST of (3.20) to

$$\overline{i^2_{w,d,eq}} \cong 4k_BT\frac{1}{2}\left(g_{m,n}\frac{\gamma}{\alpha_n} + g_{m,p}\frac{\gamma}{\alpha_p}\right). \tag{3.50}$$

The power spectral density of the MOST output conductance (3.23) is also modified to

$$\overline{i^2_{w,g_{ds},eq}} = 4k_BT\frac{1}{2}\left(\frac{g_{m,n}}{A_{i,n}} + \frac{g_{m,p}}{A_{i,p}}\right). \tag{3.51}$$

The power spectral density of the inductor and the varactor, (3.26), turns to be now

$$\overline{i^2_{w,L_{ind}}} + \overline{i^2_{w,C_{var}}} = 4k_BT\left(g_{m,n}\left(\frac{1}{2k_{osc}} - \frac{1}{2A_{i,n}}\right) + g_{m,p}\left(\frac{1}{2k_{osc}} - \frac{1}{2A_{i,p}}\right)\right) \tag{3.52}$$

Gathering together (3.50), (3.51) and (3.52), the new equivalent white noise spectral density of the LC-VCO is

$$\begin{aligned}
\overline{i^2_{w,VCO}} &= 4k_BT\left(\frac{1}{2}\left(g_{m,n}\frac{\gamma}{\alpha_n} + g_{m,p}\frac{\gamma}{\alpha_p}\right)\right. \\
&\quad \left. + \left(\frac{g_{m,n}}{2A_{i,n}} + \frac{g_{m,p}}{2A_{i,p}}\right) + \left(\frac{g_{m,n}}{2k_{osc}} + \frac{g_{m,p}}{2k_{osc}} - \frac{g_{m,n}}{2A_{i,n}} - \frac{g_{m,p}}{2A_{i,p}}\right)\right) \\
&= 4k_BT\left(g_{m,n}\left(\frac{\gamma}{2\alpha_n} + \frac{1}{2k_{osc}}\right) + g_{m,p}\left(\frac{\gamma}{2\alpha_p} + \frac{1}{2k_{osc}}\right)\right) \\
&= 4k_BT\left(g_{m,n}\xi_n + g_{m,p}\xi_p\right).
\end{aligned} \tag{3.53}$$

where $\xi_{n(p)}$ is

$$\xi_{n(p)} = \frac{\gamma}{2\alpha_{n(p)}} + \frac{1}{2k_{osc}} \tag{3.54}$$

Finally, substituting (3.53) in (3.17), the new $1/f^2$ phase noise zone equation is

$$\mathcal{L}_{1/f^2}(\Delta f) = 10\ log\left(k_B T \frac{\pi^2}{32}\frac{1}{Q^2}\Gamma_{rms}^2\left(\xi_n \frac{g_{m,n}}{I_D} + \xi_p \frac{g_{m,p}}{I_D}\right)\frac{1}{I_D}\frac{f_0^2}{\Delta f^2}\right). \tag{3.55}$$

3.3.3 $1/f^3$ region phase noise

For the general model, expression (3.35) remains

$$\frac{\overline{i_{1/f}^2}}{\Delta f} = \frac{1}{2}\left(\frac{K_{F,n} g_{m,n}^2}{C'_{ox} W_n L} + \frac{K_{F,p} g_{m,p}^2}{C'_{ox} W_p L}\right)\frac{1}{f} \tag{3.56}$$

Substituting (3.56) and (3.32) into (3.18) and rearranging terms, the phase noise in the $1/f^3$ region as function of the g_m/I_D of the transistors is:

$$\mathcal{L}_{1/f^3}(\Delta f) = 10\ log\left(\Gamma_{av}^2 \frac{\pi^2}{16^2}\frac{1}{L}\left(\frac{K_{F,n}}{C'_{ox} W_n}\left(\frac{g_{m,n}}{I_D}\right)^2 + \frac{K_{F,p}}{C'_{ox} W_p}\left(\frac{g_{m,p}}{I_D}\right)^2\right)\frac{1}{Q^2}\frac{f_0^2}{\Delta f^3}\right) \tag{3.57}$$

3.3.4 Design methodology flow

For the general approach, the design flow can be made to minimize the phase noise or the drain current. The one we present here studies the first case, but it can be developed identically for the current minimization. As the transconductances of nMOS and pMOS transistors are not equal, it complicates the design flow respect to the simplified approach. In this case, what we suggest is to pick only the inductance value L_{ind} and the g_m/I_D ratio of the nMOS transistor. Then, for each pair $\left((g_m/I_D)_n,\ L_{ind}\right)$, we have to find the $(g_m/I_D)_p^*$ that minimizes the phase noise among all of them not exceeding the maximum current I_{Dmax}. To limit the search range we propose a thirty percent away from $(g_m/I_D)_n$, that is $(g_m/I_D)_p \in (g_m/I_D)_n \cdot [0.7, 1.3] = \Psi_{n,30\%}$.

For the referred $(g_m/I_D)_p$ ratio, C_{var}, $f_{c,1/f^3}$, A_{out} and I_D are computed using (3.4), (3.39) and (3.46) and (3.49). The corresponding flow diagram is represented in Fig. 3.24, and it is organized as follows:

Step 1) Start fixing a set of initial parameters and limits: minimum transistor channel length L_{min}, the grid for Ψ, safety margin factor k_{osc}, maximum equivalent inductance $L_{ind,max}$, minimum varactor capacitance $C_{var,min}$

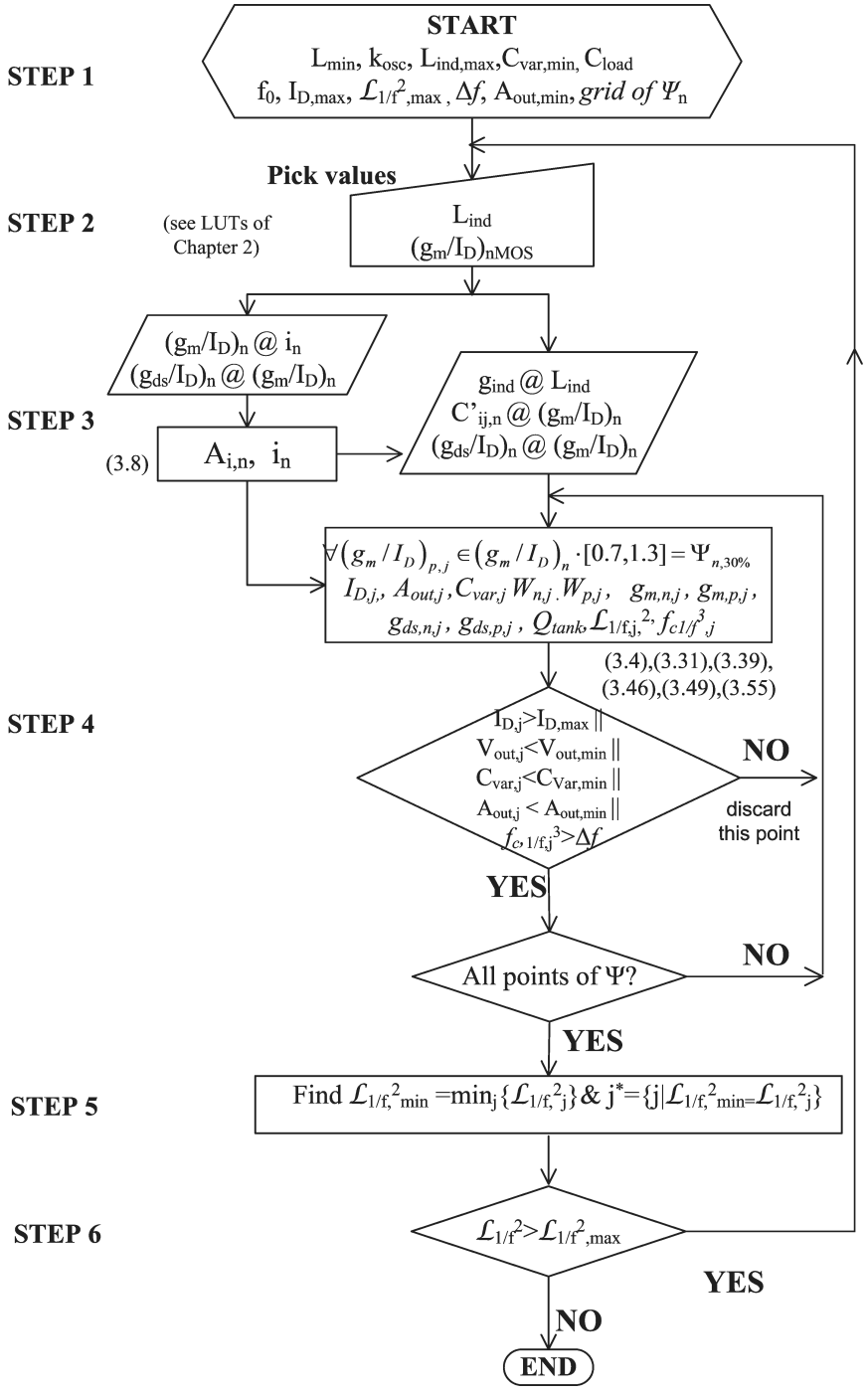


Figure 3.24: *Flow diagram for the differential LC-VCO design with the general approach.*

and C_{load}. Next, set the VCO specifications: oscillation frequency f_0, maximum current $I_{D,max}$, maximum phase noise in the white noise zone $\mathcal{L}_{1/f^2,max}$ at an offset Δf and minimum output voltage amplitude $A_{out,min}$.

Step 2) Pick a pair of values of inductor L_{ind} and $(g_m/I_D)_n$ ratio, from the technological database of inductors and transistors, which is assumed previously collected.

Step 3) From the inductor database $\Lambda_L^{(p)}$, derive the g_{ind} of that inductor. Obtain the normalized currents of nMOS, i_n, as well as $(g_{ds}/I_D)_n$, from the picked $(g_m/I_D)_n$ and the nMOS characteristic curves (g_m/I_D vs. i) and (g_{ds}/I_D vs. g_m/I_D). Calculate the intrinsic gain $A_{i,n}$ from (3.8). Extract the nMOS transistors equivalent capacitance C_{nMOS}, from the $C'_{ij,n}$ vs. g_m/I_D LUTs.

Step 4) Select any value $(g_m/I_D)_{p,j}$ of $\Psi_{n,30\%}$, and obtain the normalized current of pMOS i_p, the $(g_{ds}/I_D)_{p,j}$ and the pMOS transistors equivalent capacitance with the $C'_{ij,p}$ from the pMOS transistor LUTs. From (3.49), calculate the drain current $I_{D,j}$. Then, compute $W_{n,j}$ and $W_{p,j}$ from $I_{D,j}$, $i_{n,j}$ and $i_{p,j}$. Calculate $A_{out,j}$ from (3.46) and $C_{var,j}$ from (3.4). Compute $g_{ds,n,j}$, $g_{ds,p,j}$, $Q_{tank,j}$ with (3.31) and $\mathcal{L}_{1/f^2,j}$ from (3.55).

Calculate $f_{c,1/f^3,j}$ using (3.39), if $f_{c,1/f^3,j} > \Delta f$ or $A_{out,j} < A_{out,min}$ discard this design point and return to *Step 4* to another j. If finishing covering all the elements of Ψ go to ***Step 5***.

Step 5) From all the valid $(g_m/I_D)_p$ found in *Step 4*, look for the $(g_m/I_D)_p$ that minimizes the phase noise.

Step 6) If $\mathcal{L}_{1/f^2} > \mathcal{L}_{1/f^2,max}$ return to ***Step 2***, otherwise the design is finished.

- **Design maps**

The design flow of Section 3.3.4 is implemented in MATLAB computational routines, considering the constraints of $I_{D,max}$=0.9 mA, $C_{var,min}$=40 fF and $A_{out,min}$=0.250 V. Choosing the minimum phase noise optimization condition, the maps of Fig. 3.25 are obtained. Figure 3.25.(a) shows the $(g_m/I_D)_p$ surface map versus $(g_m/I_D)_p$ and L_{ind}. As expected, the routine chooses the minimum available $(g_m/I_D)_p$ for each $(g_m/I_D)_n$; i.e. for $(g_m/I_D)_n$=15 V^{-1}, the $(g_m/I_D)_p$=10.5 V^{-1}, except when the constraints are not met and it increases up to 14 (for low inductors). In Fig. 3.25.(b) and (c) the contour maps of the phase noise and the current are visualized. Comparing these figures with Fig. 3.7, Fig. 3.8 and Fig. 3.12 it is evident the lower values of phase noise (approximately 2 dB less) and higher current values (around 100 μA higher), reached with this general approach.

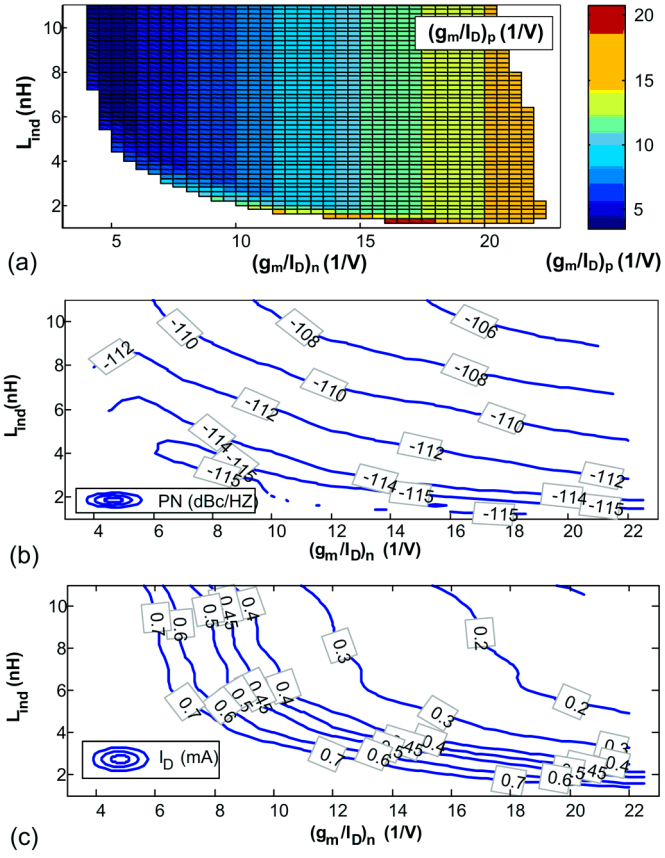


Figure 3.25: *General approach maps with phase noise minimization for $I_{D,max}$=0.9 mA, $C_{var,min}$=40 fF and $V_{out,min}$=0.25 V:(a) $(g_m/I_D)_p$, (b) Phase noise and (c) I_D versus $(g_m/I_D)_n$ and L_{ind}.*

3.4 All-nMOS/all-pMOS LC-VCO methodology

After having developed the design methodologies for the cross-coupled differential LC-VCOs, is it very simple to transform them to consider the characteristics of the all-nMOS or all-pMOS VCOs. Lets consider now the case of the all-nMOS LC-VCO, shown in Fig. 3.1.(b) as the pMOS case is identical. The previous set of equations are transformed into this new one, in which the oscillation frequency expression of (3.1) continues to be valid. The oscillation conditions is

$$k_{osc} g_{tank}^{'} = \frac{g_{m,n}}{2}. \tag{3.58}$$

Here, the tank capacitance is

$$C_{tank}^{'} = C_{var} + \frac{C_{nMOS}}{2} + C_{load} \tag{3.59}$$

with C_{nMOS} defined in (3.6). The tank conductance is:

$$g_{tank}^{'} = g_{ind} + g_{var} + \frac{g_{ds,n}}{2}. \tag{3.60}$$

Considering $A_{i,n}$ defined in (3.8), we change $k_{osc}^{'}$ by $k_{osc}^{''}$:

$$k_{osc}^{''} = \left(\frac{1}{2k_{osc}} - \frac{1}{2A_{i,n}}\right) \tag{3.61}$$

Neglecting g_{var}, (3.12) and (3.13) are still valid.

Considering the $1/f^2$ phase noise zone and the model presented in Section 3.2.3 and applying the correspondent simplifications to equations (3.20), (3.23), the all-nMOS LC-VCO white noise power spectral density remains:

$$\frac{\overline{i_{w,VCO}^2}}{\Delta f} = 4k_B T g_m \left(\frac{\gamma}{2\alpha_n} + \frac{1}{2k_{osc}}\right) = 4k_B T g_m \xi_n \tag{3.62}$$

Now we have the following phase noise expression

$$\mathcal{L}_{1/f^2}^{'}(\Delta f) = 10\ log\left(k_B T \frac{\pi^2}{32} \xi_n \frac{1}{Q^2} \Gamma_{rms}^2 \left(\frac{g_m}{I_D}\right)_n \frac{1}{I_D} \frac{f_0^2}{\Delta f^2}\right) \tag{3.63}$$

The valid design flow is the one presented for the simplified modeling of the LC-VCO in 3.2.7. What change in the diagram are the equations to be used: C_{tank} by $C_{tank}^{'}$ -(3.4) to (3.59)-, g_{tank} by $g_{tank}^{'}$ -(3.5) to (3.60)-and $\mathcal{L}$ by $\mathcal{L}^{'}$ -(3.33) to (3.63)-.

3.5 Conclusions

In this chapter we presented the third and four steps of our RF design methodology (exposed in Chapter 1) for cross-coupled LC-VCOS. Initially, a study of the differential LC-VCO architecture is done, describing it either with a simplified and a general approach. In both cases its key equations were adjusted to express them as functions of the g_m/I_D ratio. Next, a design methodology flow is proposed for each case, which, starting from the constraints and specifications and going through the modeling equations of the VCO, the elements sizing, the power consumption and the phase noise are get.

We show graphically the design compromises with respect to the inversion region or the inductor choice. We corroborate that designing in moderate and weak inversion leads to a current reduction and a phase noise increment; on the other hand an increment of the inductor value (and hence a raise in its parasitic parallel resistance) contributes to an improvement in the VCO spectral purity.

The design methodology proposed is verified with a measured prototype, which shows good agreement between measurements, simulated values and computed results in the design flow.

Finally a modification to the simplified methodology of the differential LC-VCO is proposed to cover LC VCOs with: (1) different values for g_m/I_D for the pMOS and nMOS transistors, and (2) all-nMOS or all-pMOS LC VCOs.

3.A Appendix A: Hajimiri's linear time variant phase noise theory

The theory of Hajimiri and Lee revises two hypothesis presented in the well-known and empirical theory of Leeson [Lees 66]: the linearity and the time invariance. The first hypothesis is maintained despite oscillator is itself a non-linear system because its signal amplitude is limited. The relation between the noise and the excess phase is reasonably assumed to be linear, if it is considered that the imposed perturbations are small compared with the main oscillation. The second hypothesis is lifted, as it is an erroneous assumption, because it can be easily demonstrated (see [Lee 00]) that depending on the time the noise is injected it is the resultant disturbance in the phase. As this disturbance occurs periodically, the LC-VCO is defined as a periodical linear-time-variant system.

The excess phase $\Delta\phi$ generated by a current impulse is directly proportional to the ΔV generated at the output. A current impulse at the input of the tank at the instant τ generates a change in the charge of the tank capacitor C_{tank} without any change in the inductor current. Then a Δq in C_{tank} generates a $\Delta V = \Delta q/C_{tank}$. Then, $\Delta\phi$ is:

$$\Delta\phi = \Gamma(\omega_0\tau)\frac{\Delta V}{V_{max}} = \Gamma(\omega_0\tau)\frac{\Delta q}{q_{max}} \tag{3.64}$$

where V_{max} is the maximum voltage of the capacitor, q_{max} is the maximum charge of C_{tank} and $\Gamma(\cdot)$ is a new function defined in this theory, called impulse sensitivity function (ISF). It describes the sensitivity to the system to an impulse injected at a phase $\omega_0\tau$. This function depends on the system and it differs from LC-VCOs to ring VCOs, to mention an example. The ΔV and Δq have to be normalized respect to the maximum voltage or charge of the capacitor to maintain the proportionality relation between phase and voltage, without having units.

In order to understand the effect of the phase noise in these circuits the excess phase response $h_\phi(t)$ to unit charge impulse $u(t)$ at instant τ is

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau) \tag{3.65}$$

For an input current $i(t)$, the excess phase can be calculated by

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau)i(\tau)d\tau = \frac{1}{q_{max}}\int_{-\infty}^{t} \Gamma(\omega_0\tau)i(\tau)d\tau \tag{3.66}$$

As $\Gamma(\cdot)$ is a periodical function it can be expressed by Fourier series with coefficients c_n:

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n cos(n\omega_0\tau + \theta_n) \tag{3.67}$$

where c_n are real and θ_n is the phase of the *nth* harmonic of the ISF. The phase θ_n is ignored because it is assumed that the noise components are uncorrelated and their relative phase have no meaning [Lee 00]. Then, substituting (3.67) into (3.66) and considering known these c_n coefficients, the excess phase is:

$$\phi(t) = \frac{1}{q_{max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau)d\tau\right] \tag{3.68}$$

Last expression models the known VCO feature that a noise of a particular frequency injected into an oscillator produces spectral components at other frequencies. To demonstrate this property, $i(t)$ is considered to be a sinusoidal current source with phase $(m\omega_0 + \Delta\omega)t = 2\pi(mf_0 + \Delta f)t$, where mf_0, with m integer positive, is a frequency multiple of the oscillator frequency and, as it has been used in this chapter, $\Delta f << f_0$. All the integrals of the terms in (3.68) are negligible except when n=m. Finally, the excess phase noise results in the following approximated expression:

$$\phi(t) \approx \frac{I_m c_m \sin(\Delta\omega t)}{2q_{max}\Delta\omega} \tag{3.69}$$

It shows that the spectrum of $\phi(t)$ are two impulses at $\pm\Delta\omega$, despite the spectrum of the imposed signal is at frequency $m\omega_0 + \Delta\omega$.

However, in the VCO design, what is needed is the spectrum of the output signal voltage. A phase-to-voltage mechanism exists and it is the modulation of the excess phase ϕ that appears in the output signal. If the output voltage is considered to be sinusoidal, this phase modulation appears because $V_{out}(t) = A_{out}cos(\omega_0 + \phi(t))$. Then, from (3.16) and (3.69) [Lee 00], the expression of phase noise can be written as

$$\mathcal{L}(\Delta f) \approx 10log\left(\frac{I_m c_m}{2q_{max}\Delta\omega}\right)^2 \tag{3.70}$$

This result can be extended to a white noise source with a psd equal to $\overline{i_w^2}$

$$\mathcal{L}(\Delta f) \approx 10log\left(\frac{\overline{i_w^2}(c_0^2/2 + \sum_{n=1}^{\infty} c_n^2)}{4q_{max}^2\Delta\omega^2}\right) \tag{3.71}$$

This expression shows another oscillator feature, the fact that the noise around the harmonics of the oscillator frequency is downconverted to the baseband in the excess phase generation. This is, in fact, the spectrum of the $1/f^2$ region; and it can be rewritten using Parseval's theorem ($c_0^2/2 + \sum_{n=1}^{\infty} c_m^2 = 2\Gamma_{rms}^2$) as function of Γ_{rms}^2

$$\mathcal{L}(\Delta f) = 10\ log\left(\frac{\Gamma_{rms}^2\overline{i_w^2}}{2q_{max}^2\Delta\omega^2}\right) \tag{3.72}$$

For the flicker noise, where we consider at first approximation that only the term weighted by c_o remains, (3.71) is transformed into

$$\mathcal{L}(\Delta f) = 10\ log\Big(\frac{\overline{i_{1/f}^2}c_o^2}{8q_{max}^2\Delta\omega^2}\Big) = 10\ log\Big(\frac{\overline{i_{1/f}^2}\Gamma_{av}^2}{2q_{max}^2\Delta\omega^2}\Big) \tag{3.73}$$

with $\overline{i_{1/f}^2}$ the flicker noise source psd and $\Gamma_{av} = c_0/2$.

CHAPTER 4

LNAs design methodology

LOW NOISE AMPLIFIERS, or LNAs, are one of the fundamental blocks of a receiver, either as stand-alone circuits [Le 09, Chen 08, Do 10, Xuan 10, Joo 09] or as a cell in a interwoven subsystem e.g. the LNA-mixer-VCO cell of [Lisc 06] or the LNA-mixer cell of [Amer 07]. The adequate design of this block is crucial to reach good receiver performance. It is mainly because the level of LNA noise determines the ability of the system to recognize a very low power input signal. Of course, other amplifier characteristics beyond the low noise could make a receiver not to achieve its specifications of gain, power consumption, area or even linearity. In addition, an LNA has to be designed to have good input and output matching with its adjacent circuits -noise and/or impedance matching, depending on the application-.

The objective of this chapter is to complete the design methodology we have been presenting in Chapters 1 and 2, for LNAs. It will permit the resolution of LNA sizing and characteristics in a short period of time with little effort on the designer's part. This method helps the designer to know in advance the LNA behavior when certain basic parameters are swept. As it has been mentioned in Chapter 2, to perform these studies, we will use the g_m/I_D ratio as the basic tool together with the MOS transistor bias current I_D. These two variables permit to explore the design space of a specific set of LNA features and component characteristics, particularly: noise figure, gain, values and dimensions of inductances and capacitances and transistor widths (as the transistor length is considered fixed to the minimum of the technology).

As we have introduced in Chapter 1, the circuits considered in this dissertation are aimed to be used in low-power, short-range and low-rate radiofrequency (RF) applications existent nowadays, unified in standards, such as ZigBee or low-energy Bluetooth. For the LNA optimization methodology presented here, it is translated in reducing as much as possible the circuit power consumption, always below pre-established limits, and complying with the LNA specifications. In particular, special emphasis is made here on developing the optimization methodology that obtains, for each bias current and each inversion level of the MOST, the minimum noise figure available.

This chapter pays special attention in demonstrating the need of good MOS transistor noise parameters models so that the final LNA noise figure computations

tally with the simulations and measurements. We have observed that not including the phase noise parameter variations with the MOS transistor inversion regions generates appreciable differences between the computed and the SpectreRF simulated data, being more noticeable in moderate and weak inversion.

We study two LNA topologies in this chapter: (1) the common-source LNAs (CS-LNAs), which is the most popular LNA architecture; and (2) the common-gate LNA (CG-LNAs).

Another contribution of the work is the inclusion of the flicker noise in the analytical computation of the noise figure of the LNA. We have noticed that for some technologies, the contribution of flicker noise cannot be neglected when compared with the white noise at radio-frequencies. Not adding the corresponding term of flicker noise in the noise figure expression could lead to errors, especially in strong and moderate inversion.

As the implemented LNAs are usually biased through a choke resistor, we studied the influence of this device in the LNA noise figure and gain.

This chapter is organized as follows. Section 4.1 presents the CS-LNA optimization methodology, which includes a review of the previously proposed CS-LNA optimization techniques in Subsection 4.1.1; the signal and noise modeling in Subsection 4.1.2; the details of the CS-LNA design methodology flow based on g_m/I_D ratio in Subsection 4.1.3; the validation of the method via twelve CS-LNA designs in Subsection 4.1.4; and finally the measurements of a fabricated 2.4-GHz CS-LNA in the TECH1 technology, designed with the proposed method, in Subection 4.1.5. Subsequently, Section 4.2 presents a sketch of the CG-LNA design methodology. Finally, Section 4.3 summarizes the main contributions of this chapter.

4.1 CS-LNA optimization methodology

This section presents the noise figure-power consumption optimization methodology for common-source LNAs (CS-LNAs), which schematic is shown in Fig. 4.1. The trade-offs between three of the main CS-LNA characteristics, the noise figure, the power gain and the power consumption, are thoughtfully studied, due to the impact of these figures in the rest of the RF system. The optimization is done principally by means of taking advantage of the current consumption-current noise trade-off of the LNA, forcing the design to consume just the needed current to fulfill the specifications. As it has been presented in Chapter 2, the basis of the optimization is the use of the g_m/I_D technique and MOS transistor all-inversion regions.

As we will show afterwards, the g_m/I_D tool allows us to reduce power consumption for a given set of specifications, which, in the case of the LNA are the noise figure (NF) and the gain (G). The fundamental idea is to reach the LNA specifications without an unnecessary low noise figure much below the specifications, as a low noise figure generally entails a waste of power. It is expected that in moderate inversion, where low power consumption is reached, an acceptable noise figure could be obtained. This last fact highlights the importance of having a design methodology which covers the complete spectrum of the inversion zones.

To develop this design methodology, four general steps, as presented in Chapter 1, should be followed: 1) the DC behavior of MOS transistor has to be captured

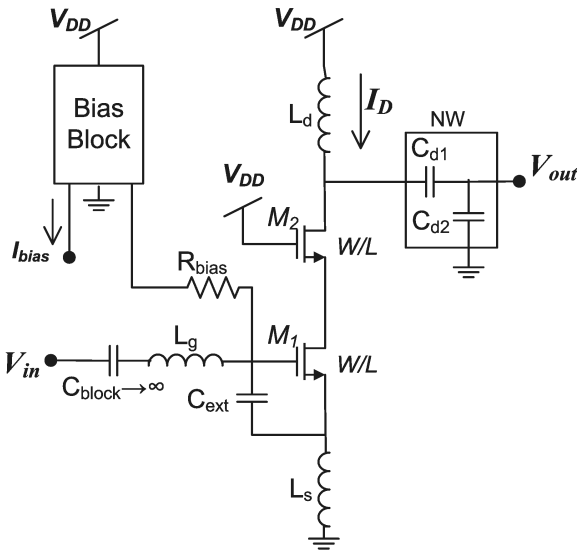


Figure 4.1: *Schematic of the single ended CS-LNA used to describe the methodology proposed.*

in curves or expressions, basically, of g_m/I_D versus i, and g_{ds}/I_D and intrinsic capacitances versus g_m/I_D. This requires a MOS transistor model accurately characterized in all-operation regions as we have described in Section 2.1; 2) the extraction of passive component models (Section 2.3); 3) the modeling of the CS-LNA with an equation set, and 4) it is necessary to establish a design flow to arrange the computations, the application of the technological data collected in the two first steps, and the relations between them and the decisions fixed by the LNA specifications and technological constraints. These two last steps will be detailed in Sections 4.1.3 and 4.1.4.

4.1.1 Review of CS-LNA optimization techniques

Several works have dealt with LNAs design optimization, presenting various techniques which contribute to solve this problem. This part of the chapter presents the most significant ones. In 1997 Shaeffer and Lee [Shae 97] presented one of the first published studies of LNA optimization methods specifically focused on CMOS technologies. In this work, the authors considered computing the noise figure (in which it is added the induced gate noise) considering as variables the input network quality factor Q_L and the parameter $\rho = V_{OD}/(Lv_{sat})$ which depends on the overdrive voltage $V_{OD} = V_{GS} - V_T$, the MOS transistor length L and the saturation velocity v_{sat}. Two optimization procedures were shown, where the design is constrained by fixing either the amplifier equivalent transconductance G_m or amplifier power consumption P_D; always relating the noise figure with V_{OD}. This approach is very appealing but lacks of some important considerations: 1) it only covers the strong inversion region as the expression of ρ is only valid in this region; 2) the amplifier transconductance does not include the resistive term of the gate inductor. Not considering MI and WI limits the possibilities of reducing power consumption; and neglecting gate inductor resistances -which in Chapter 2 were proven not to be small for high inductances- generates a sub-optimized design. Finally in this work the common source architecture used did not decouple the noise from the current consumption, i.e: to reduce the noise, the bias current must increase.

An improvement in the CS-LNA architecture -the addition of C_{ext}, a capacitor between gate and source-has been lately introduced by Andreani and Sjöland in [Andr 01], allowing the reduction of noise in LNAs without the need of raising power. This work maintains the idea of Shaeffer and Lee of working in strong inversion region, taking again the input network quality factor as a variable of optimization, but it is chosen, instead of ρ, the transistor width W. It calculates the optimum W and with it, the optimum power consumption, either for short or long channel transistors, varying Q_L. Again, inductor parasitics are not considered.

Next, Nguyen et al. [Nguy 04] summarize the most important techniques to

design an LNA: a) noise matching[1], b) noise and input matching [2], c) power constraint noise optimization and d) power constraint simultaneous noise and input matching; all consistent among them. This study is very helpful to give the designer a clear understanding of the design principles, fundamental limitations and advantages of the four methods, based on the noise figure equations. However, the transistor is again studied only in strong inversion and no inductor parasitics are added in the equation set. Also, the election of the external capacitor C_{ext} for the last technique is somewhat arbitrary and it is not a practical approach.

The work of Belostotsky and Haslett in [Belo 06] improves in many aspects the abovementioned works. It takes into consideration the finite quality factor of the inductors, in particular the gate inductor and integrates the sizing of the external capacitor C_{ext} in the optimization flow. This work uses the technique of input impedance matching, considering that the noise impedance is similar to the input impedance and the design will be near the minimum noise figure value (as discussed in the work of Lee, [Lee 04], Section 12.3). The optimization technique presented by the authors has two optimization approaches, which can be mixed together: gain and/or power constrained noise optimization. The gain constrained approach means to limit the amplifier transconductance value, and to vary the input network quality factor. The power constrained approach is the same as the one presented by Shaeffer and Lee. When both restrictions apply, optima C_{ext} and ρ (or V_{OD}) are found numerically. Nevertheless, this work does not include a study of moderate and weak inversion. On the other hand, when the constraints are set to gain and power, the authors independently determine the parasitic series resistance and the inductance value of the gate inductor. Following this method, designing an inductor with such characteristics for a certain technology would be somewhat difficult to achieve.

Our contribution goes one step beyond [Belo 06], by adding five new features. The first and most important is the coverage of all-inversion regions, which has been discussed since the beginning of this dissertation. Secondly, it uses real inductors taken from the technology involved (in this case TECH1) throughout the design flow, particularly for the gate and drain inductor. This simplifies enormously the identification of the best technology inductor to use, without waisting time and resources, and even discarding the possibility of not finding the right one and finally designing a under-optimized LNA. In third place, it considers the noise parameters as function of g_m/I_D, i.e. as function of the MOS transistor inversion regions, due to their notorious effects on the design. Finally, the flicker noise and the noise due to the bias resistor choke R_{bias} are included in the noise figure computation. As

[1] Noise matching is reached when the input impedance is adjusted to an optimum impedance to obtain the minimum noise figure [Lee 04].

[2] Input matching is obtained when the LNA input impedance Z_{in} is matched to the impedance of the source Z_s.

far as we know, there are no published works that analytically consider the flicker noise in LNA designs, probably due to the belief that in high frequencies flicker noise is insignificant respect to white noise, which is not always true. The same happens with the study of the effect of the R_{bias}, which up to what we know, it has not been analytically presented in published works (it has been considered in [Belo 08] but not included analytically). When there is no other way to bias the LNA than with a resistance, since area limitations forbid the use on-chip inductors, the effects in the LNA noise figure and in the gain have to be undoubtedly studied. We show how for small values of R_{bias} these characteristics worsen.

The first approach of our LNA methodology was made in [Fior 08b, Sens 09], where the initial considerations of the design methodology as well as the design of a moderate/weak inversion LNA in the 90nm ST technology were presented. The advances of our study were presented in [Fior 11b] and are fully discussed in this chapter.

4.1.2 Signal and noise modeling

In this section we present the principal relations between gain, noise and matching specifications and the elements of the topology. We obtain a power constrained noise optimized CS-LNA design, using the input matching technique [Nguy 04, Belo 06]. Our work shares the initial ideas formulated in [Belo 06]. All-inversion regions are studied and a simple, yet systematic optimization methodology is presented. Moreover, we add two effects not considered previously in an analytical way in LNA studies, as previously mentioned. One is the inclusion of α and γ variations with the g_m/I_D, which affects the LNA noise figure, especially in moderate and weak inversion regions. The other is the analytical inclusion of the flicker noise in the noise figure calculation, because for some technologies, this noise would be substantially large and noticeable yet above the gigahertz. Finally, power gain and noise figure are deduced for matched input and output networks LNA constraints.

In order to describe the proposed methodology, the inductively degenerated common source low noise amplifier of Fig. 4.1 is utilized. The LNA includes an external gate-source capacitor C_{ext} to provide the already mentioned degree of freedom in the design. The amplifier stage is composed by the gate inductor L_g, the source inductor L_s, capacitor C_{ext} and the MOS transistor amplifier M_1. The cascoded transistor M_2 decouples input and output signals and increases the output impedance. The output matching network comprises the drain inductor L_d and a capacitive network NW, C_{d1} and C_{d2}. The Bias Block contains a scaled copy of M_1 and generates the corresponding voltage in the node of R_{bias}. Input and load impedances, R_s and R_L, are assumed real. The cascoded transistor M_2 has been considered equal to M_1, to simplify the deduction of the design methodology.

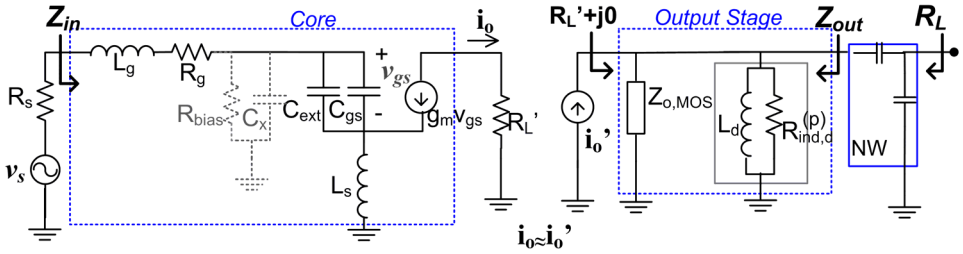


Figure 4.2: *Small-signal model for the CS-LNA of Fig. 4.1.*

In this work, the small-signal model considered for that topology is depicted in Fig. 4.2. The parasitic series resistance of the gate inductor, $R_{ind,g}^{(s)}$, and the extrinsic gate resistance of the MOST, $R_{g,MOS} = \frac{R_{\square} W}{(12 \cdot n_f^2 \cdot L)}$, with $R_{\square}$ the gate sheet resistance and n_f the number of fingers, are considered, gathered together as R_g. The parasitic resistance of the source inductor, the gate-bulk C_{gb} and the gate-drain C_{gd} parasitic capacitances as well as R_{bias} are discarded in equations (4.1) to (4.10) for the sake of facilitating the explanation, as the expressions are considerably simplified. Second order effects due to R_{bias}, C_{gb} and C_{gd} are presented at the end of this Section. Cascode M_2 transistor effect is only included in the core output impedance $Z_{o,MOS}$, which simplified expression is sketched in Appendix 4.A, therefore the output current of the transistor $M1$, i_o, is considered to be equal to the input current of LNA output stage, $i_o^{'}$.

Input stage analysis

Defining $C_t = C_{gs} + C_{ext}$, the CS-LNA input impedance is

$$Z_{in}(s) = R_g + sL_g + sL_s + \frac{1}{sC_t} + L_s \frac{g_m}{C_t} \tag{4.1}$$

Assuming matching impedance at f_0 between the CS-LNA input and the purely resistive input voltage source, the following expressions for real and imaginary part of (4.1) are obtained

$$R_s = R_g + L_s \frac{g_m}{C_t} \tag{4.2}$$

and

$$0 = \omega_0^2 (L_g + L_s) C_t - 1. \tag{4.3}$$

Solving (4.2) and (4.3) for unknowns L_s and C_t, results

$$C_t = \frac{g_m L_g}{2R} \left(\sqrt{1 + \frac{4R}{g_m L_g^2 \omega_0^2}} - 1 \right) \tag{4.4}$$

and

$$L_s = \frac{C_t}{g_m} R \tag{4.5}$$

with $R = R_s - R_g$. Defining $R_t = R_s + R_g$, the input stage effective transconductance evaluated at ω_0 is

$$G_{eff} = |G_{eff}(j\omega_0)| = \left|\frac{i_o}{v_s}\right| = \frac{g_m}{\omega_0\left(R_t C_t + L_s g_m\right)} = \frac{R/R_s}{2\omega_0 L_s}. \tag{4.6}$$

Output stage analysis

In order to do the LNA power transfer as efficient as possible, the output stage has to be designed so that the effective load of the core block is resistive ($R_L^{'} + j0$) and with a high value. Since in general the output impedance of the core, $Z_{o,MOS}$ is capacitive, ($Im(Z_{o,MOS}) < 0$), we use the drain inductor L_d, to compensate both its imaginary part and to produce a purely inductive output impedance of the LNA, Z_{out}, that via the capacitive network NW it can be coupled to the resistive output load R_L. Although this impedance transformation is achieved by minimizing the drain inductor value and this optimizes the area of design, on the contrary, the parallel parasitic resistance, $R_{ind,d}^{(p)}$, also reduces (see Fig. 2.25) which implies a reduction in the value of output power or equivalently the LNA power gain. Thus, the drain inductor value is a trade-off value between the above two conditions: acceptable area and high power gain. For the impedance transformation that takes place in the output stage through the capacitive network NW, it must be verified that

$$Re(Z_{out}) < R_L, \quad Im(Z_{out}) > 0. \tag{4.7}$$

These conditions imply the following maximum value for the drain inductor,

$$L_{d,max} = \frac{1}{\omega_0\left(\sqrt{G_{out}(1/R_L - G_{out})} + Im(1/Z_{o,MOS})\right)} \tag{4.8}$$

where the LNA output conductance is

$$\begin{aligned} G_{out} &= Re\left(\frac{1}{Z_{out}}\right) = Re\left(\frac{1}{Z_{o,MOS}} + \frac{1}{j\omega_o L_d} + \frac{1}{R_{ind,d}^{(p)}}\right) \\ &= Re\left(\frac{1}{Z_{o,MOS}}\right) + \frac{1}{R_{ind,d}^{(p)}}. \end{aligned} \tag{4.9}$$

Equation (4.7) can be viewed graphically with the Smith diagram presented in Fig. 4.3, considering R_L=50 Ω. Z_A is $Z_{o,MOS}$, which is capacitive, and hence it is

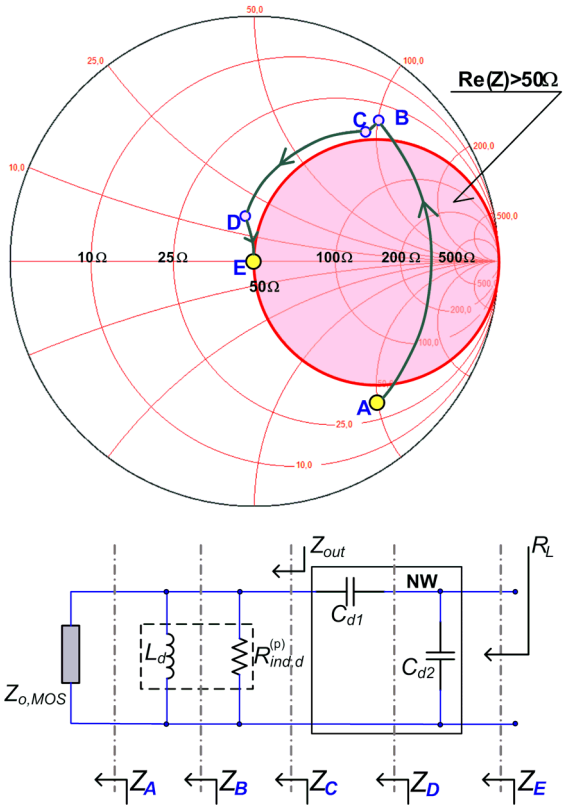


Figure 4.3: *Smith diagram showing the impedance changes when each output component is added.*

located in the negative plane of the Smith Chart in (A). Then, when $L_d < L_{d,max}$ is added , dot (A) is translated to the positive plane to dot (B), being Z_A transformed to Z_B, with $Re(Z_B)$ <50 Ω. A minor correction due to $R^{(p)}_{ind,d}$ moves dot (B) to dot (C); Z_C=Z_{out} and $Re(Z_C) = Re(Z_{out})$<50 Ω and $Im(Z_{out} > 0)$, obeying (4.7). Then, the serial capacitor of the output network *NW* C_{d1} moves dot (C) to dot (D) around the circle of $Re(Z_C)$ <50 Ω. Finally, capacitor C_{d2} of *NW* adjusts the impedance of dot (D) to dot (E), hence, Z_D to Z_E=50Ω=R_L. If dot (C) is inside the circle of $Re(Z) > 50$, no combination of capacitors in *NW* can translate (C) to R_L=50 Ω.

From (4.9) the power gain G is

$$G = 10log\left(\frac{P_{out}}{P_{in}}\right) = 10log\left(\frac{i_o^2}{4G_{out}} / \frac{v_s^2}{4R_s}\right) = 10\ log\left(\frac{|G_{eff}|^2 R_s}{G_{out}}\right). \qquad (4.10)$$

Noise modeling analysis

The total noise factor of the CS-LNA of Fig. 4.2, F, has two contributors: the noise factor of the core block and the noise factor of the output stage. Since the cascode transistor noise is lower than that of the amplification transistor [Shae 97], it has not been included in the core noise factor.

In general, the works that analytically study LNAs do not include flicker noise current into the MOS drain current noise equation as it is generally negligible respect to the white noise current value at the working frequency. However, this simplification is not always valid since some CMOS technologies have flicker noise levels non negligible with respect to to white noise values, especially in SI and MI. Therefore, we include here the flicker noise current density in the noise figure computations.

The expression of the total noise factor F is expressed as the noise factor due to the core, F_{core} plus the term of the output stage, F_{OS}, as follows

$$F = 1 + (F_{core} - 1) + (F_{OS} - 1). \tag{4.11}$$

The noise factor of the core F_{core}, is

$$F_{core} = \frac{\overline{i_{s,o}^2} + \overline{i_{R_g,o}^2} + \overline{|i_{ng,o} + i_{nd,o}|^2}}{\overline{i_{s,o}^2}} \tag{4.12}$$

where $i_{s,o}$ and $i_{R_g,o}$ are the output noise currents due to the input source and the R_g resistances; $i_{g,o}$ and $i_{d,o}$ are the output noise currents due to the induced gate noise current and drain current of MOST, respectively. From [Belo 06], F_{core} can be rewritten as follows

$$\begin{aligned} F_{core} = 1 &+ \frac{\overline{v_{R_g}^2}}{\overline{v_s^2}} + \frac{\overline{i_g^2}}{\overline{v_s^2}} \frac{|\Gamma(j\omega_0)|^2}{|G_{eff}(j\omega_0)|^2} + \frac{\overline{i_d^2}}{\overline{v_s^2}} \frac{|\Delta(j\omega_0)|^2}{|G_{eff}(j\omega_0)|^2} \\ &+ \frac{\overline{i_g i_d^*}}{\overline{v_s^2}} \frac{\Gamma(j\omega_0)\Delta(j\omega_0)^*}{|G_{eff}(j\omega_0)|^2} + \frac{\overline{i_g^* i_d}}{\overline{v_s^2}} \frac{\Gamma(j\omega_0)^*\Delta(j\omega_0)}{|G_{eff}(j\omega_0)|^2} \end{aligned} \tag{4.13}$$

where the noise power spectral density due to R_s and R_g are $\overline{v_s^2} = 4k_BTR_s$ and $\overline{v_{R_g}^2} = 4k_BTR_g$. The induced gate noise psd is given in (2.22). Finally, $\overline{i_g i_d^*} = -\overline{i_g^* i_d} = j|c|\sqrt{\overline{i_g^2}\,\overline{i_d^2}}$, where c is the correlation coefficient given in (2.23). In this work both white noise and flicker noise current psd of (2.20) and (2.21) are considered in the drain noise current psd.

$$\overline{i_{nd}^2} = 4k_BTg_m\frac{\gamma}{\alpha} + \frac{K_F g_m^2}{C'_{ox}WLf}. \tag{4.14}$$

The functions $\Delta(j\omega_0)$ and $\Gamma(j\omega_0)$ describe, respectively, the transfer relations from drain noise, i_d, and gate noise, i_g, current sources to the output current i_o [Belo 06]. Their values are

$$\Delta(j\omega_0) = R_t/2R_s, \tag{4.15}$$

$$\Gamma(j\omega_0) = \frac{R_t + j\omega_0(L_s+L_g)}{2R_s}\frac{g_m}{j\omega_0 C_t}. \tag{4.16}$$

Being $\overline{i^2_{G_{out}}} = 4k_BTG_{out}$ the noise power spectral density of the output conductance G_{out}, the output stage noise factor F_{OS} is

$$F_{OS} = \frac{\overline{i^2_{s,o}} + \overline{i^2_{G_{out,o}}}}{\overline{i^2_{s,o}}} = 1 + \frac{\overline{i^2_{G_{out}}}}{\overline{v_s^2}G^2_{eff}} = 1 + \frac{G_{out}}{R_sG^2_{eff}} = 1 + 10^{-G/10}. \tag{4.17}$$

Transfer function from G_{out} noise current source, $i_{G_{out}}$, to the output current, i_o, is the unity.

Finally, the LNA noise figure NF is

$$NF = 10\ log(F) \tag{4.18}$$

The noise factor expressions considering the addition of the R_{bias}, C_{gd} and C_{gb} are presented in the following section.

- **Inclusion of C_{gd}, C_{gb} and R_{bias} in the modeling**

When R_{bias} and/or C_{gd} and C_{gb} are considered in the LNA equations, the input impedance as well as L_s and C_t have complicated expressions. Therefore, in order resolve the matching network condition $Z_{in}(j\omega_0) = R_s + j0$, we will use a perturbed expression [Bend 99] of L_s and C_t with the perturbative parameters $\varepsilon_1 = R/R_{bias} = R\ G_b$ and $\varepsilon_2 = C_xL_g\omega_0^2$, with $C_x = 2C_{gd} + C_{gb}$, which must verify $\varepsilon_1 << 1$, $\varepsilon_2 << 1$.

The effective impedance Z_{eff} from v_s is

$$Z_{eff}(s) = \frac{v_s}{I_{in}} = \frac{D(s)}{A(s)} \tag{4.19}$$

where

$$\begin{aligned} D(s) &= 1 + s(R_tC_t + g_mL_s) + s^2C_t(L_g + L_s) \\ &\quad + \Big(R_t + s(L_g + g_mR_tL_s) + s^2(R_tC_tL_s + g_mL_gL_s) + s^3C_tL_gL_s\Big)(G_b + sC_x), \\ A(s) &= sC_t + (1 + sg_mL_s + s^2C_tL_s)(G_b + sC_x). \end{aligned} \tag{4.20}$$

Matching conditions over the effective impedance produce the following set of equations to solve

$$\begin{aligned} Re(Z_{eff})|_{j\omega_0} &= 2R_s, \\ Im(Z_{eff})|_{j\omega_0} &= 0, \end{aligned} \tag{4.21}$$

If we assume first order perturbations for the unknowns

$$\begin{aligned} C_t &\approx C_t^{(0)} + \varepsilon_1 C_t^{(1)} + \varepsilon_2 C_t^{(2)} \\ L_s &\approx L_s^{(0)} + \varepsilon_1 L_s^{(1)} + \varepsilon_2 L_s^{(2)}. \end{aligned} \tag{4.22}$$

We get, from (4.21), the solutions

$$\begin{aligned} C_t^{(0)} &= \frac{g_m L_g}{2R}\left(\sqrt{1+4R/(g_m L_g^2\omega_0^2)}-1\right) \\ L_s^{(0)} &= C_t^{(0)} R/g_m \\ C_t^{(1)} &\approx \frac{1-2g_mR}{g_m L_g \omega_0^2 R} + \frac{5g_mR-4}{g_m^2 L_g^3 \omega_0^4} \\ L_s^{(1)} &\approx -\frac{L_g}{g_m R} + \frac{2-g_mR}{g_m^2 L_g \omega_0^2} \\ C_t^{(2)} &\approx -\frac{1}{L_g\omega_0^2} + \frac{(g_mR+1)R}{g_m L_g^3 \omega_0^4} \\ L_s^{(2)} &\approx \frac{R}{g_m L_g \omega_0^2} + \frac{(g_mR-1)R^2}{g_m^2 L_g^3 \omega_0^4}. \end{aligned} \tag{4.23}$$

To compute the total gain using (4.10), the new expression of the effective transconductance is needed. The first order approximation using the obtained solutions of (4.23) is

$$|G_{eff}(j\omega_0)| = \left|\frac{g_m}{D(j\omega_0)}\right| \approx \frac{R/R_s}{2\omega_0 L_s^{(0)}}\left(1 - \frac{1-g_mR}{g_mR_{bias}} - \frac{R^2C_x}{L_g}\right) \tag{4.24}$$

To correct the total noise figure of the transistor, the transfer function $\Delta(s)/G_{eff}(s)$ has to be reevaluated and a new function $H_b(s)/G_{eff}(s)$ has to be added. $H_b(s)$ represents the transfer function from R_{bias} noise voltage source, $v_{R_{bias}}$, to the output current, i_o. The transfer function $\Gamma(s)/G_{eff}(s)$ has been reevaluated but as the variation due to R_{bias} and /or C_x perturbations is minimal, it is not considered here.

Thus, the first order correction of $\left|\frac{\Delta}{G_{eff}}\right|^2_{j\omega_0}$ is

$$\left|\frac{\Delta}{G_{eff}}\right|^2_{j\omega_0} \approx \left(\frac{R_t\omega_0 L_s^{(0)}}{R}\right)^2\left(1 + \left(\frac{L_g^2\omega_0^2}{R_s^2-R_g^2} + \frac{1-2g_mR}{g_mR}\right)2\varepsilon_1 + \frac{R^2}{L_g^2\omega_0^2}2\varepsilon_2\right) \tag{4.25}$$

and the term to add to the core noise factor expression (4.12), due to R_{bias}, is

$$F_{core}(R_{bias}) = \frac{\overline{i^2_{R_{bias},o}}}{\overline{i^2_{s,o}}} = \frac{\overline{v_{R^2_{bias}}}}{\overline{v^2_s}} \left| \frac{H_b(j\omega_0)}{G_{eff(j\omega_0)}} \right|^2$$
$$= \frac{R_{bias}}{R_s} \left| \frac{g_m(R_t + sL_g)(G_b + sC_x)/D(s)}{g_m/D(s)} \right|^2_{s=j\omega_0}$$
$$= \frac{R_t^2 + \omega_o^2 L_g^2}{R_s} \left(\frac{1}{R_{bias}} + \omega_0^2 R_{bias} C_x^2 \right). \quad (4.26)$$

4.1.3 Design methodology flow

Having obtained the power gain, input impedance matching and noise factor as functions of the MOS transistor model and noise parameters, this section presents the proposed design flow that optimize the noise figure, considering a power consumption constraint. Its objectives are the correct biasing and sizing of the MOS transistors and the sizing of L_g, L_s, L_d and C_{ext}. In order to facilitate the comprehension of the method, in this section we use the expressions (4.1) to (4.10), considering that R_{bias}, C_{gb} and C_{gd} do not affect the design. When we computationally implement the method with MATLAB we use the complete method with all the effects included in Section 4.1.2.

The design flow covers all the possible pairs (I_D,g_m/I_D) with I_D below the maximum acceptable $I_{D,max}$. For each pair, the main two steps are the following: first, find the drain inductor included in $\Lambda_L^{(p)}$ which minimizes the output conductance, G_{out}, and second, find the gate inductor included in $\Lambda_L^{(s)}$ that minimizes NF.

Following the above ideas, the methodology flow diagram, presented in Fig. 4.4, is organized in the following steps.

Step 1) Start by setting the constraints of a minimum transistor length L_{min} and the inductor LUTs $\Lambda_L^{(s)}$ and $\Lambda_L^{(p)}$, and the specifications: working frequency f_0, load R_L, a maximum transistor bias current I_{Dmax}, a maximum noise figure NF_{max} and, a minimum power gain G_{min} .

Step 2) Pick a pair of I_D and g_m/I_D values, using the transistor technology database, which is assumed previously collected.

Step 3) With the pair (g_m/I_D, I_D), and the transistor technology database (characteristic curves g_m/I_D vs. i, g_{ds}/I_D vs. g_m/I_D and C'_{ij} vs. g_m/I_D) obtain the normalized current i, the transistor width W, the output conductance g_{ds}, an estimation of $R_{g,MOS}$ (choosing the maximum n_f to have the lowest value) and C_{gs}. Calculate $Z_{o,MOS}$ and $L_{d,max}$ from (4.47), (4.48) and (4.8).

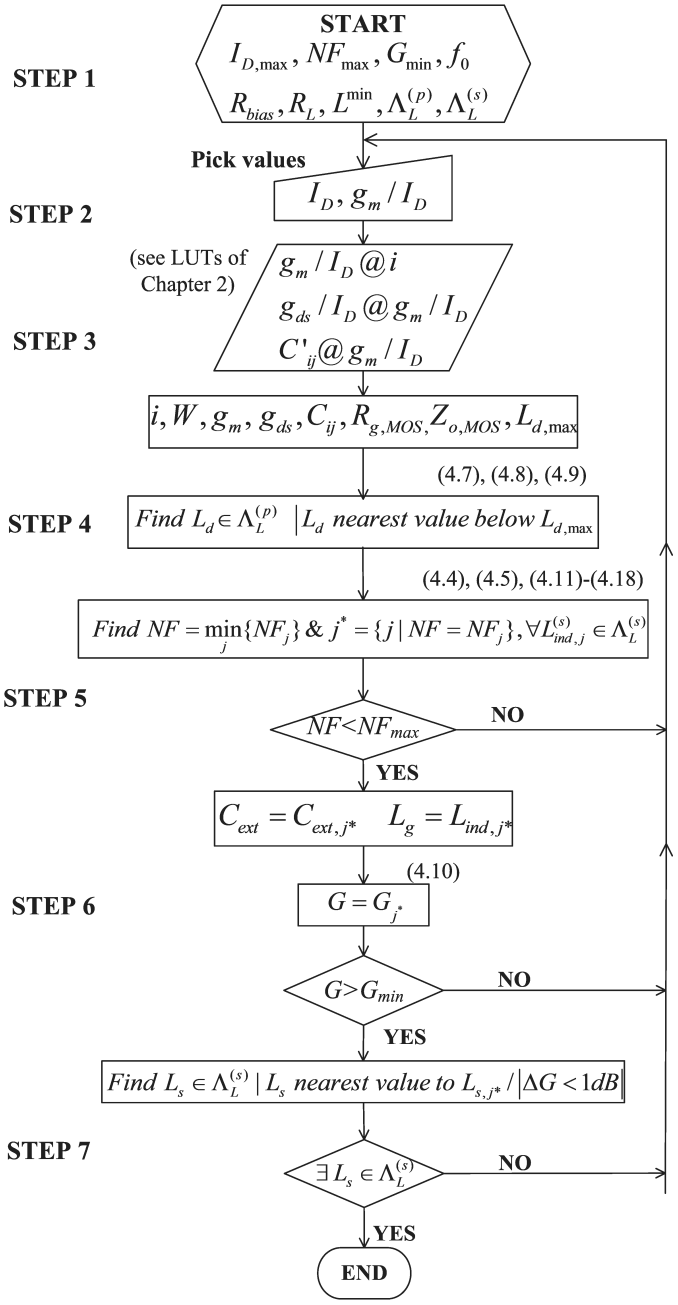


Figure 4.4: *Diagram flow of the proposed LNA design methodology.*

Step 4) Being $L_{d,max}$ the computed drain inductance, find the drain inductor L_d in the LUT $\Lambda_L^{(p)}$, as that with the nearest inductance below $L_{d,max}$. This condition produces the lowest G_{out} and allows to find a capacitive network NW up to R_L.

Step 5) Now, as a possible gate inductor L_g, pick each inductor $L_{ind,j}^{(s)}$ of $\Lambda_L^{(s)}$. Extract its serial resistance $R_{ind}^{(s)}$ and apply (4.4), (4.5) and (4.11) to (4.18) to obtain $C_{ext,j}$, $L_{s,j}$ and NF_j. Then, the j^* index at which the lowest value of NF is reached, is chosen for the final gate inductor. Then $L_g = L_{ind,j^*}^{(s)}$, $C_{ext} = C_{ext,j^*}$.

If NF is higher than NF_{max} return to Step 2), otherwise continue.

Step 6) Compute the gain G using (4.10). If G is lower than G_{min}, return to Step 2) and choose another (g_m/I_D, I_D).

Step 7) Being L_{s,j^*} the computed source inductance, find the nearest inductor in the LUT $\Lambda_L^{(s)}$ that produces a variation in power gain less than 1 dB. If no inductor exists, return to Step 2). Otherwise, the design is finished.

If L_s differs from the calculated L_{s,j^*}, the gain of the final circuit would excessively vary from the calculated one, due to (4.6) and (4.10). Then, if it is admitted a maximum power gain variation (in dB), $\Delta G = |G_{L_s} - G_{L_{s,j^*}}|$, using (4.6) and (4.10), it is deduced that

$$\Delta G = |-20\Delta(logL_s)| \tag{4.27}$$

and specifically $\Delta G = |20log(L_{s,j^*}/L_s)|$. For example, for ΔG=1 dB, with L_{s,j^*}=0.5 nH, the feasible tolerance for L_s is 0.06 nH; and for L_{s,j^*}=10 nH, the tolerance grows up to 1.15 nH. Expression (4.27) justifies the use of the logarithmic grid of 20 points per decade in the generation of the LUTs.

In order to assess the performance of this design flow, we have implemented it in MATLAB computational routines. In this way, we visualize the characteristics of the CS-LNA parameters as well as its component sizing for the available ranges of g_m/I_D and I_D, and then depict them in contour maps. Particularly, noise figure and power gain are plotted in Fig. 4.5; and C_t and L_s are presented in Fig. 4.6, considering g_m/I_D varying between 5 V^{-1} and 22 V^{-1} and I_D between 100 μA and 1.5 mA. The database obtained from the TECH1 is employed. The following values are fixed: f_0=2.445 GHz, L_{min}=100 nm, R_{bias}=10 kΩ, R_s=R_L=50 Ω.

Figure 4.5.(a) presents the noise figure versus g_m/I_D for four drain current values; and in Fig. 4.5.(b) the noise figure design space is presented as contour maps. In both graphs, one of the LNA key trade-offs is visible here: the compromise of noise figure versus consumption, since as expected, the noise figure decreases

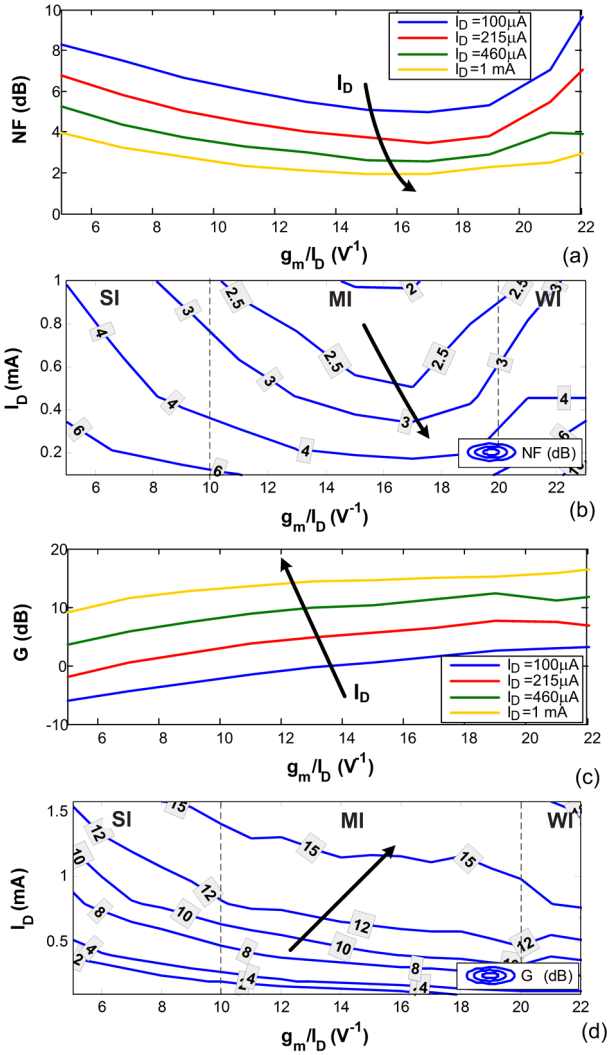


Figure 4.5: *(a) and (c) Optimized noise figure and power gain versus g_m/I_D for four drain current values. (b) and (d) Optimized noise figure and power gain contour maps.*

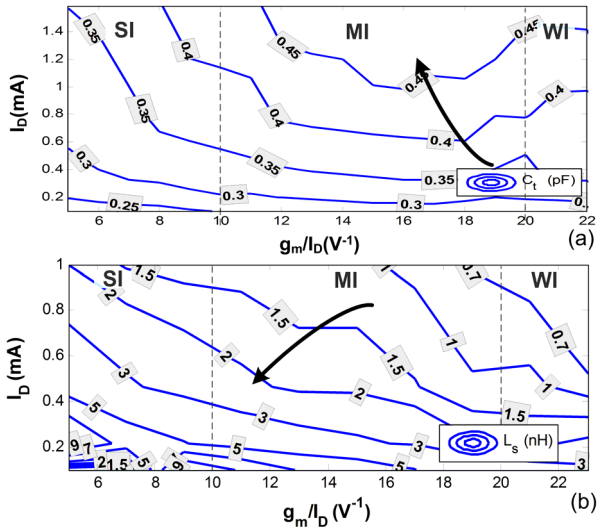


Figure 4.6: *Optimized (a) C_t and (b) L_s versus I_D and g_m/I_D. The three inversion regions are highlighted.*

for high current values. In particular, an optimum design area is visualized in the moderate inversion region which covers $g_m/I_D \in [14, 19]\ V^{-1}$.

Figure 4.5.(c) shows the power gain versus g_m/I_D for four current values; and Fig 4.5.(d) the contour maps of the power gain are presented. These graphs show the expected increment in the gain when the drain current increases and the gain raises when moving through weak inversion. The increment in the gain when moving to weak inversion is due to the fact that the gain is inversely proportional to L_s, due to (4.6), and L_s has a decreasing behavior when moving through weak inversion, as shown in Fig. 4.6.(b) and explained next.

To complete this study, C_t and L_s are depicted in the maps of Fig. 4.6.(a) and

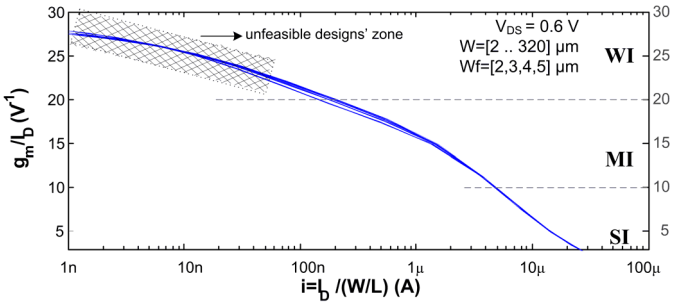


Figure 4.7: *g_m/I_D versus i for TECH1, where the area painted in grey stands for the CS-LNA unfeasible zone.*

Fig. 4.6.(b). L_g contours are similar to the ones of L_s but are not shown here. This behavior occurs because for a fixed g_m/I_D the normalized current i must remains constant due to the one-to-one relation g_m/I_D vs i. When I_D raises, at the same proportion MOST width W raises as well, and so happens to C_t. Then, due to (4.3), to maintain a constant ω_0 the inductances must decrease.

Finally, lets present again in Fig. 4.7 the g_m/I_D ratio versus i for this technology TECH1, where it is drawn a shadowed region in the weak inversion zone. In this region, the LNA designs are unfeasible due to the impossibility of design such small source inductors for this technology.

4.1.4 Validation by simulation

We validate the proposed design technique presented in previous sections by the electrical simulation of twelve CS-LNAs in the same conditions of the previous examples, referred as {PSi, PSMi, PMi, PWi}, with i={1,2,3} in Fig. 4.8 and Table 4.1. We consider three current values (1.4 mA, 0.9 mA, 0.4 mA) as well as four possible inversion regions by varying the $g_m/I_D(V^{-1})$ from 6 (SI), 11 (SI-MI), 15 (MI) up to 20 (WI). Particularly, Table 4.1 presents the LNA components sizing, noise figure and gain calculated via the computational routines that implement the design flow of Fig. 4.4. It also presents the noise figure and power gain obtained with SpectreRF simulations, using in them the components sizing obtained previously. Comparing the SpectreRF simulations and the numerical computations using the CS-LNA presented methodology, similar results are appreciated, with differences of less than 1 dB in the power gain and 0.6 dB in the noise figure.

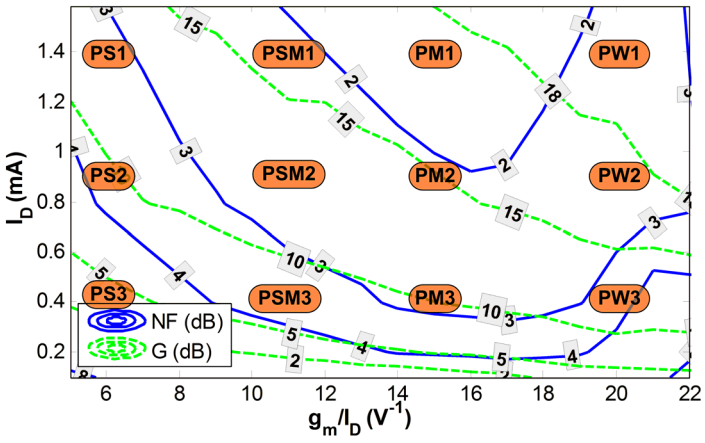


Figure 4.8: *Design space map of NF and G vs I_D and g_m/I_D for R_{bias}=10kΩ. The chosen designs are also shown.*

Table 4.1: *Method validation: comparison between computational routines and SpectreRF simulations.*

Design	g_m/I_D (1/V)	I_D (mA)	W (μm)	C_t (fF)	C_{ext} (fF)	L_s (nH)	L_g (nH)	L_d (nH)	G (dB)		NF (dB)	
									Calc.	Sim.	Calc.	Calc.$_{w/o\ 1/f}$	Sim.
PS1	6	1.4	12.3	353.1	338.7	1.2	10.6	11.1	12.7	11.9	3.1	2.5 (19%)	3.4
PS2	6	0.9	8.0	334.6	324.2	1.9	10.6	11.1	9.6	8.8	3.7	3.0 (19%)	4.1
PS3	6	0.4	3.6	300.4	299	4.1	9.6	11.1	3.7	2.7	5.0	4.1 (18%)	5.6
PSM1	11	1.4	35.7	432.3	392.6	1.0	8.7	11.1	15.7	15.3	2.1	1.7 (19%)	2.3
PSM2	11	0.9	22.9	409.1	383.5	1.4	8.8	11.1	12.8	12.3	2.4	2.0 (18%)	2.7
PSM3	11	0.4	10.2	341.9	330.5	2.4	9.6	11.1	7.8	7.0	3.5	2.9 (17%)	3.7
PM1	15	1.4	96.3	479.4	381.8	0.8	7.9	11.1	16.4	17.0	1.7	1.6 (6%)	1.8
PM2	15	0.9	61.9	426.9	364.2	1.1	8.7	11.1	14.4	14.2	2.0	1.8 (10%)	2.1
PM3	15	0.4	28.4	361.4	331.8	2.0	9.5	11.1	9.7	9.3	2.8	2.5 (11%)	2.9
PW1	20	1.4	320	458.2	179.9	0.5	8.7	6.6	16.9	15.9	2.1	2.0 (5%)	2.0
PW2	20	0.9	320	407.3	129	0.7	9.6	7.2	14.9	13.6	2.4	2.3 (2%)	2.4
PW3	20	0.4	205.3	330.2	151.7	1.1	11.6	9.6	11.5	9.5	3.5	3.4 (1%)	3.2
	Inputs		Calculated parameters						Specification results				

To show the need of adding the flicker noise term, in the column that lists the computed noise figure without considering the flicker noise (Calc.$_{w/o\ 1/f}$) the relative error made has been added. As expected, the highest errors values appear in SI and MI, as the transistor sizes are smaller than in WI, showing its effect. Notice that these data confirm the need for adding the flicker noise term in the noise figure expression.

4.1.5 Experimental validation

The experimental validation of the LNA design methodology proposed in this work is done by presenting a 2.4-GHz differential CS-LNA implemented in TECH1 to be used in a fully differential ZigBee receiver. The total power consumption and noise figure were limited to 1.8 mW and 5 dB respectively. The gain must be higher than 9 dB and the IIP3 higher than -5 dBm for input and output impedances of 50 Ω. To design a differential circuit based on the proposed method, we obtain the single-ended design following the design flow of Fig. 4.4; then we mirror the circuit to generate a differential structure. In our differential LNA we employ a differential symmetric source inductor with its center tap connected to ground and since the L_s calculated by the procedure is single ended we use the double of this value to find a differential inductor included in the technology set. This procedure was not done for L_d as the double of the computed value is not feasible in the TECH1 technology.

Due to area constraints we had to use an R_{bias}=1 kΩ instead of R_{bias}=10 kΩ.

Table 4.2: *Differential CS-LNA component and specification values comparison for Matlab and SpectreRF simulations.*

Characteristics		Calc.	Schem.	Post-layout
I_D (μA)		570	570	570
g_m/I_D (V^{-1})		17.4	17.4	17.4
L_s (nH)		1.1	1.1	0.75
L_g (nH)		9.6	9.6	11.1
L_d (nH)		10.5	10.5	10.5
W_{M_1}(μ m)		92.8	92	92
C_{gs} (fF)		88	92	92
C_{ext} (fF)		300	270	240
G (dB)	R_{bias}=10kΩ	12.6	12.3	-
	R_{bias}=1kΩ	11.1	10.7	10.3
NF (dB)	R_{bias}=10kΩ	2.3	2.5	-
	R_{bias}=1kΩ	3.8	3.85	4.35
IIP3		–	-5	-3.5

This reduces by ten times the occupied area by the resistor and, due to the smaller size, R_{bias} could be laid-out very near to the MOS transistor; a bigger sizing would oblige us to place it far from the MOST, increasing considerably the layout capacitive parasitics in the MOST gate, reducing the C_{ext} value; thus non controlling correctly the effective external gate capacitance. This force us to re-run the design flow utilizing this new value, entailing an acceptable increment in the noise figure of the design. Table 4.2 presents the computation results together with the schematic simulation and the post-layout simulations. The data are presented for the two R_{bias} values to observe the differences. The table shows very good matching between the computational data and the results from schematic simulations. The sizing adjustments of L_g, L_s and C_{ext} in the post-layout simulation are due to the compensation of layout parasitics of the routing and the pads capacitances. The final schematic of this differential LNA is shown in Fig. 4.9, where the Bias Block is composed by a pMOS mirror and a scaled nMOS M_{1b} to copy the generated current to transistors M_1.

The microphotograph of the implemented LNA is shown in Fig. 4.10. The circuit covers an area of 0.91 mm^2 (845 μm $\times$ 1080 μ m) without considering pad area. The LNA characterization has been made on chip, using a Cascade RF microprobe station. S-parameter measurements were performed with the Agilent N5230 Two-ports Network Analyzer and power gain and IIP3 were measured with the Agilent E4440A Spectrum Analyzer. Noise figure was measured with the Ag-

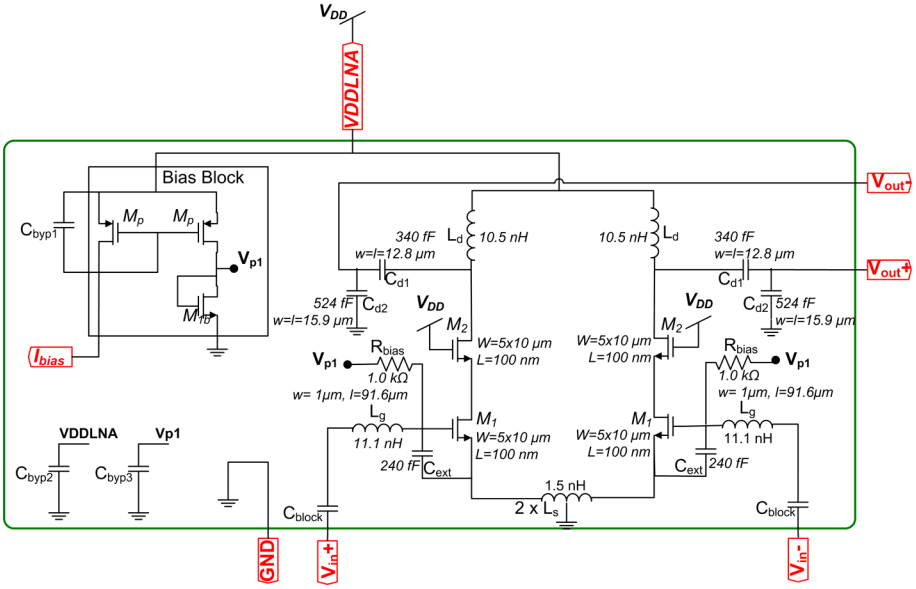


Figure 4.9: *Final schematic of the fabricated Differential LNA.*

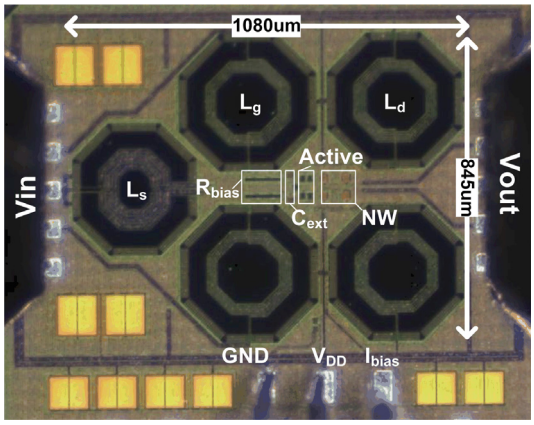


Figure 4.10: *Microphotograph of the differential CS-LNA. The active area as well as the passive components are marked.*

ilent N8974A Noise Figure Analyzer. As all our equipment is single-ended, we were able to do only single-ended measurements, inferring by symmetry, a similar behavior for the differential scheme.

The measured S-parameters are shown in Fig. 4.11 in the band between 2.0 GHz and 2.8 GHz. The input and output networks resonant frequencies have a shift down of 180 MHz and 110 MHz, respectively, visualized when traces S_{11} and S_{22} minimize ($|S_{11}| < -20\ dB$ and $|S_{22}| < -20\ dB$). These shifts reduce the gain and increase the NF in the band of interest. The LNA gain is equal to 9.7 dB at 2.445 GHz exceeding the specifications of 9 dB; but is approximately 0.6 dB less than the expected 10.3 dB of post-layout simulated results, an expected difference due to corner variations. The LNA isolation is correct, as $|S_{12}|$ is below -35 dB (not shown).

Figure 4.12 depicts the noise figure in the band between 2.0 GHz and 2.8 GHz, with a minimum of 3.9 dB. At 2.445 GHz it achieves 4.36 dB, very near of the expected value.

The input third order intermodulation point (IIP3) as well as the 1-dB compression point (P1dB) were measured. The P1dB is found to be -9 dBm. Figure 4.13 plots the measured amplitude of the fundamental and third order intermodulation spur when two tones separated 1 MHz, with variable amplitude, were injected. Extrapolating, the IIP3 value is -4 dBm. In the inset of Fig. 4.13 it is shown a sample of the output spectrum of the two tone input signals.

Finally the input second order intermodulation point (IIP2) was measured by injecting two tones at 2.445 GHz$\pm$1.25 MHz (2.44625 GHz and 2.44375 GHz), so the second order intermodulation tone falls in the baseband frequency of 2.5 MHz. Extrapolating, the IIP2 value is 61 dBm, as shown in Fig. 4.14.

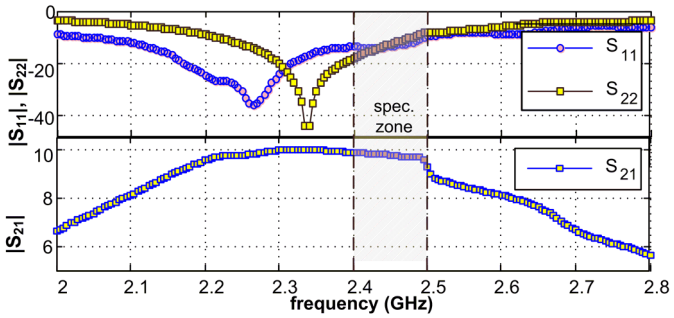


Figure 4.11: *Measured modulus S-parameters of the fabricated CS-LNA: $|S_{11}|$ and $|S_{22}|$ (above), and $|S_{21}|$ (below). The ZigBee band is shadowed.*

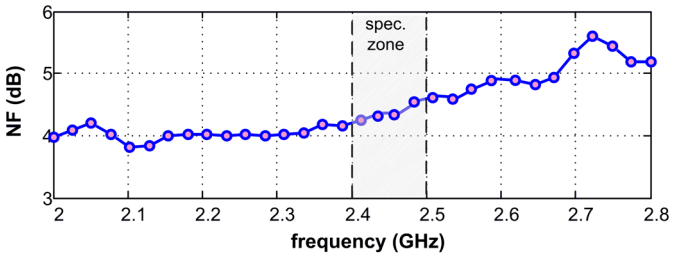


Figure 4.12: *Noise figure measurements in the 2.0 GHz-2.8 GHz band, where the ZigBee band is shadowed.*

Comparison with other works

Table 4.1.5 compares the performance of the designed CS-LNA in moderate inversion with that of some prior works, utilizing a figure of merit usually applied to LNAs [ITRS 09]

$$FoM = (G \cdot IIP3 \cdot f)/((F-1) \cdot P_{DC}) \tag{4.28}$$

where G is the power gain in dB, IIP3 is in mW, f is the working frequency in GHz, F is the noise factor, and P_{DC} is the total power in mW. As observed, our differential CS-LNA is well positioned considering other similar designs; only the work of [Sivo 05] present a bit higher FoM due to the high gain and the low noise, however this CS-LNA is not appropriate to be used in ZigBee applications due to its very high power consumption. If higher R_{bias} values would have been used these FoM would have increased even more. For example, with a 10 kΩ bias resistor we could have achieved a $FoM \approx 22$ GHz, using for these calculations the post-layout data.

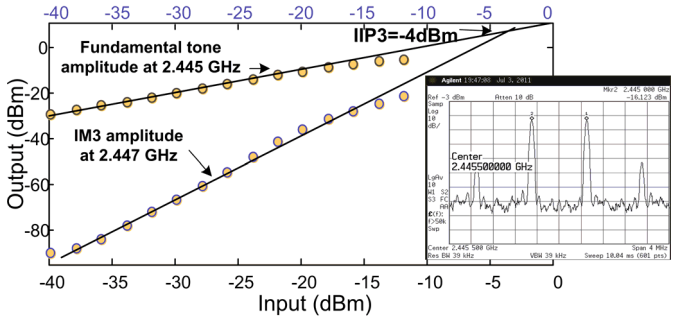


Figure 4.13: *Measured IIP3 of the differential CS-LNA and output spectrum of the principal and IM3 tones (inset).*

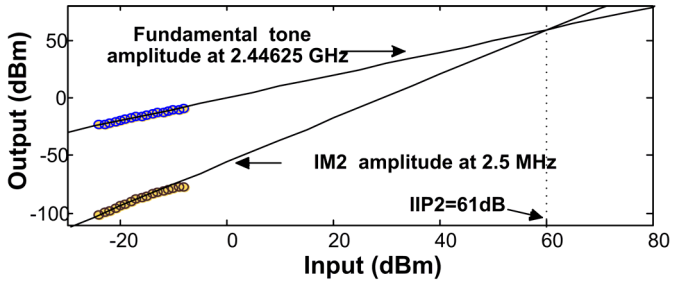


Figure 4.14: *Measured IIP2 of the differential CS-LNA.*

Table 4.3: *Performance comparison of recently published CS-LNAs.*

Source	Tech. (nm)	f_0 (GHz)	IIP3 (dBm)	P_{DC} (mW)	G (dB)	NF (dB)	FoM (GHz)
Diff. LNA[a]	90	2.445	-4	0.68	9.7	4.8	8.0
[Do 10] (2010)	180	2.4	-10	1.8[b]	14	9	0.45
[Xuan 10] (2010)	180	2.4	-2	12	15	2	3.2
[Joo 09] (2009)	130	2.4	-11	2.6	24	2	3.0
[Do 08] (2008)	180	2.4	-19	0.95	21.4	5.2	0.3
[Tzen 08] (2008)	130	2.3	-21.4	1.08	25	3.1	0.4
[Lee 06] (2006)	130	3	-11	0.4	9.1	4.7	2.8
[Sivo 05] (2005)[a]	130	2.2	-4	4.2	17.6	1.6	8.2

[a] Single-ended structure considered to normalize the comparison.
[b] Inferred values.

4.2 CG-LNA optimization methodology

The use of CS-LNA structure has been generalized due to the trade-offs encountered between gain and noise figure, the relative simplicity of the design and the amount of works which study it. However for higher frequencies or ultra wide band (UWB) solutions, the common gate LNA architecture is a very good option since its noise figure does not increase its value with the working frequency, as happens with CS-LNA; however its gain is not so high.

The first approach of our methodology was made in [Fior 08a], where the initial considerations of the design methodology for CG-LNAs in AMS 0.35μm process was studied.

This section presents a g_m/I_D based design flow of a simple CG-LNA architecture, in order to expand the proposed methodology of Chapter 1 to other LNAs architectures.

4.2.1 Signal and noise modeling

As well as we have used in the CS-LNA, this design is adjusted to be input-impedance matched. This condition can be relaxed for some implementations, especially for UWB designs [Lu 06].

The basic architecture is presented in Fig. 4.15. It consists of a common gate source-degenerated MOS transistor M_1 amplifier; its input signal is injected through the source terminal of the MOST, which is connected to the ground via the

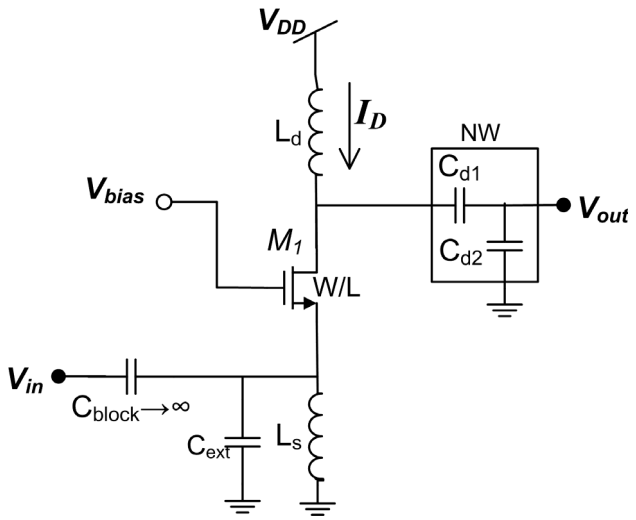


Figure 4.15: *CG-LNA schematic.*

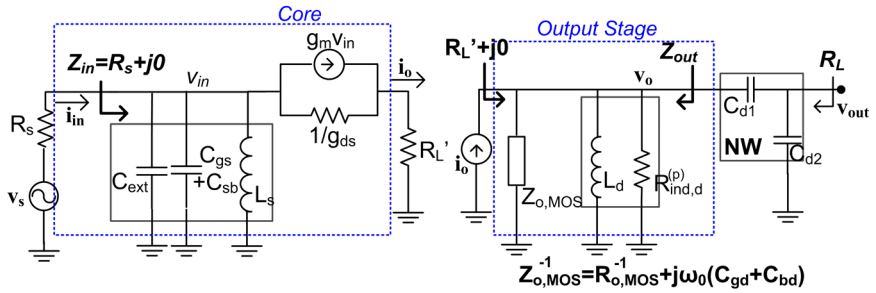


Figure 4.16: *Small-signal scheme of the CG-LNA architecture studied.*

L_s inductor. An external capacitor C_{ext} is included to facilitate the input matching condition with feasible low-value source inductor. Inductor L_d connects the supply voltage to the drain terminal of M_1 and the output network NW matches the load R_L to the output impedance of the CG-LNA. The MOS transistor biasing is adjusted by means of the DC gate voltage, which in this study it is considered an ideal source. As a first approach, the inductor L_s is chosen to have a parasitic parallel resistance at less ten times higher than the input source resistance, R_s, to neglect its effect in the circuit.

To deduce the equations that govern this architecture, lets use the small-signal schematic of Fig. 4.16, where capacitor C_{gb} does not appear as it is short-circuited. The LNA is divided into two stages, the core stage and the output stage. The core stage is composed by the MOS transistor M_1, the inductor L_s and the external capacitor C_{ext}. The output stage includes the core output impedance, $Z_{o,MOS}$, where $Z_{o,MOS}^{-1} = R_{o,MOS}^{-1} + j\omega_0(C_{gd}+C_{bd})$, the inductor L_d and its parasitic parallel resistance $R_{ind,d}^{(p)}$. $R_L^{'}$ is the load seen from i_o.

Input stage analysis

The input matching condition is $Z_{in} = R_s + j0$, hence computing Z_{in} we have

$$Z_{in}^{-1} = \frac{1}{j\omega_0 L_s} + j\omega_0(C_{ext}+C_{gs}+C_{gb}) + \frac{g_m + g_{ds}}{1+g_{ds}R_L^{-1}} = \frac{1}{R_s} + j0. \tag{4.29}$$

From the real and imaginary part of the previous equality we obtain

$$\begin{aligned} R_L^{'} &= R_s\left(1+\frac{g_m}{g_{ds}}\right) - \frac{1}{g_{ds}} \\ C_{ext} &= \frac{1}{\omega_0^2 L_s} - C_{gs} - C_{gb} \end{aligned} \tag{4.30}$$

To reach the input matching condition, $R_L^{'}$, the load seen from i_o must be fixed to the value expressed above.

The output parallel resistance of the input stage is

$$R_{o,MOS} = R_s\Big(1+\frac{g_m}{g_{ds}}\Big)+\frac{1}{g_{ds}}. \tag{4.31}$$

Output stage analysis

The output impedance Z_{out} of the output stage is

$$\begin{aligned} Z_{out}^{-1} &= \frac{1}{j\omega_0 L_d}+\frac{1}{R_{ind,d}^{(p)}}+Z_{o,MOS}^{-1} \\ &= \frac{1}{j\omega_0 L_d}+\frac{1}{R_{ind,d}^{(p)}}+R_{o,MOS}^{-1}+j\omega_0(C_{gd}+C_{bd}) \\ &= G_{out}+jB_{out} \end{aligned} \tag{4.32}$$

where

$$G_{out} = \frac{1}{R_{ind,d}^{(p)}}+\frac{1}{R_{o,MOS}}. \tag{4.33}$$

Considering that the impedance seen at the input of the output network NW must be ${Z_{out}^{*}}^{-1} = G_{out}-jB_{out}$, the input impedance $Z_L^{'}$ of the output stage is,

$${Z_L^{'}}^{-1} = \frac{1}{R_L^{'}} = j\omega_0(C_{gd}+C_{bd})+\frac{1}{j\omega_0 L_d}+\frac{1}{R_{ind,d}^{(p)}}+G_{out}-jB_{out} \tag{4.34}$$

The real and imaginary part of the previous expression are written as functions of the unknown G_{out}, B_{out} and $R_{ind,d}^{(p)}$, as follows:

$$\begin{aligned} \frac{1}{R_L^{'}} &= \frac{1}{R_{ind,d}^{(p)}}+G_{out} \\ B_{out} &= \omega_0(C_{gd}+C_{bd})+\frac{1}{\omega_0 L_d}. \end{aligned} \tag{4.35}$$

As $R_L^{'}$ is known from (4.30) we can write the unknowns G_{out} and $R_{ind,d}^{(p)}$ from (4.33) and (4.35) as

$$G_{out} = \frac{1}{2}\Big(\frac{1}{R_{o,MOS}}+\frac{1}{R_L^{'}}\Big) \tag{4.36}$$

$$\frac{1}{R_{ind,d}^{(p)}} = \frac{1}{2}\Big(\frac{1}{R_L^{'}}-\frac{1}{R_{o,MOS}}\Big). \tag{4.37}$$

If a capacitive output network NW is used, as we have explained in Section 4.1.2, the following two conditions have to be met

$$Re(Z_{out}) < R_L, \quad Im(Z_{out}) > 0. \tag{4.38}$$

These conditions imply the following maximum value for the drain inductor:

$$L_{d,max} = \frac{1}{\omega_0\left(\sqrt{G_{out}(1/R_L - G_{out})} + \omega_0(C_{gd}+C_{bd})\right)} \tag{4.39}$$

Power gain

The power gain of the CG-LNA can be written as

$$G = 10log\left(\frac{P_{out}}{P_{in}}\right) = 10log\left(\frac{i_o^2}{4G_{out}} / \frac{v_s^2}{4R_s}\right) \tag{4.40}$$

As the transfer function of i_{in} to i_o is the unity $i_o = i_{in} = v_s/(2R_s)$, then

$$G = 10\ log\left(\frac{1}{4R_sG_{out}}\right). \tag{4.41}$$

Noise figure

The noise factor F of this architecture is

$$F = 1 + (F_{core} - 1) + (F_{OS} - 1) = \frac{\overline{i^2_{LNAcore,o}}}{\overline{i^2_{s,o}}} + \frac{\overline{i^2_{Gout,o}}}{\overline{i^2_{s,o}}} \tag{4.42}$$

with $\overline{i^2_{s,o}} = (1/2)^2\overline{i^2_s}$, as the function transference between $i_{s,o}$ and i_s. Neglecting in the expression of the psd of $\overline{i^2_{LNAcore,o}}$ the noise of the conductance g_{ds} and of the induced gate noise, $\overline{i^2_{LNAcore,o}} \cong \overline{i_{nd,o}} = \overline{i_{nd}}|\Delta(j\omega_0)|^2$, with

$$\Delta(j\omega_0) = \frac{1}{1 + R_s(g_m + g_{ds}) + g_{ds}R'_L} = \frac{1}{2R_s(g_m + g_{ds})}. \tag{4.43}$$

Finally

$$\begin{aligned} F =& 1 + \frac{\overline{i^2_{nd}}|\Delta(j\omega_0)|^2}{(1/2)^2\overline{i^2_s}} + \frac{\overline{i^2_{Gout}}}{(1/2)^2\overline{i^2_s}} \\ =& 1 + \frac{\overline{i^2_{nd}}|\Delta(j\omega_0)|^2}{(1/4)\overline{i^2_s}} + 4G_{out}R_s = 1 + \frac{\overline{i^2_{nd}}|\Delta(j\omega_0)|^2}{(1/4)\overline{i^2_s}} + 10^{-G/10} \end{aligned} \tag{4.44}$$

where $\overline{i^2_{nd}} = 4k_BTg_m\frac{\gamma}{\alpha} + \frac{K_Fg_m^2}{C_{ox}^2WLf}$, $\overline{i^2_s} = 4k_BT/R_s$ and $\overline{i^2_{Gout}} = 4k_BTG_{out}$.

In this structure the effect of the gate noise is neglected respect to the other noise components, even for frequencies up to $\omega_0/\omega_T = 0.5$ [Zhuo 05]. It is not the case of a CS-LNA architecture, due to the input resonant tank that increases the gate noise contribution by its quality factor. In case this noise would be added to the equations, an interesting deduction is presented in [Lu 06].

4.2.2 Design methodology flow

With the resulting set of equations derived in the previous section, it is now possible to lay-out a design flow, similar to the one proposed for the CS-LNA architecture, as shown in Fig. 4.17. Again, the design flow covers the range of possible pairs $(g_m/I_D, I_D)$, up to a maximum $I_{D,max}$. For each pair, it is found the inductor L_s and external capacitor C_{ext} to reach the input impedance imaginary condition and R_{ext} to adjust the input impedance real condition. Then it is calculated the power gain G and the noise figure NF. The diagram flow follows the design steps listed below.

Step 1) Start by setting the constraints of a minimum transistor length L_{min} and the inductor LUT $\Lambda_L^{(p)}$, and the specifications: the working frequency f_0, the load R_L, a maximum transistor bias current I_{Dmax}, a maximum noise figure NF_{max} and and a minimum gain G_{min}.

Step 2) Pick a pair of I_D and g_m/I_D values, using the transistor technology database, which is assumed previously collected.

Step 3) Find L_s included in $\Lambda_L^{(p)}$ (see Section 2.3) whose $R_{p,s}$ is much larger than R_s, to limit the perturbation of the parasitic resistance of L_s over the input impedance seen at the source of the MOST.

With the pair (g_m/I_D, I_D), and the transistor technology database, presented in Chapter 2, obtain the corresponding normalized current i, the g_{ds}/I_D ratio and the C'_{ij}.

Using the above data compute C_{gs}, C_{gd}, C_{gb} and C_{bd}. Calculate C_{ext} and R'_L from (4.30), $R_{o,MOS}$ from (4.31), G_{out} from (4.36), $R_{ind,d}^{(p)}$ from (4.37) and $L_{d,max}$ using(4.39).

Step 4) Find the inductor L_d included in $\Lambda_L^{(p)}$ which inductance is lower than $L_{d,max}$ and parasitic parallel resistance equal to $R_{ind,d}^{(p)}$. If it does not exist return to ***Step 2***, otherwise continue.

Step 5) Compute the power gain and the noise figure using (4.41) and (4.44). If $NF > NF_{max}$ or $G < G_{min}$, return to ***Step 2***. Otherwise the flow is finished.

As it has been done in similar sections of the work, we have implemented this design flow in MATLAB computational routines, making it possible to observe the behavior of the design variables in contour maps. As initial values there have been considered $f_0 = 2.445$ GHz, L_{min}=100 nm, $R_s = R_L$=50Ω.

Figure 4.18.(a) presents the noise figure design space versus g_m/I_D and I_D. It is observed an optimum NF zone, along the line of the arrow. Also, for high currents,

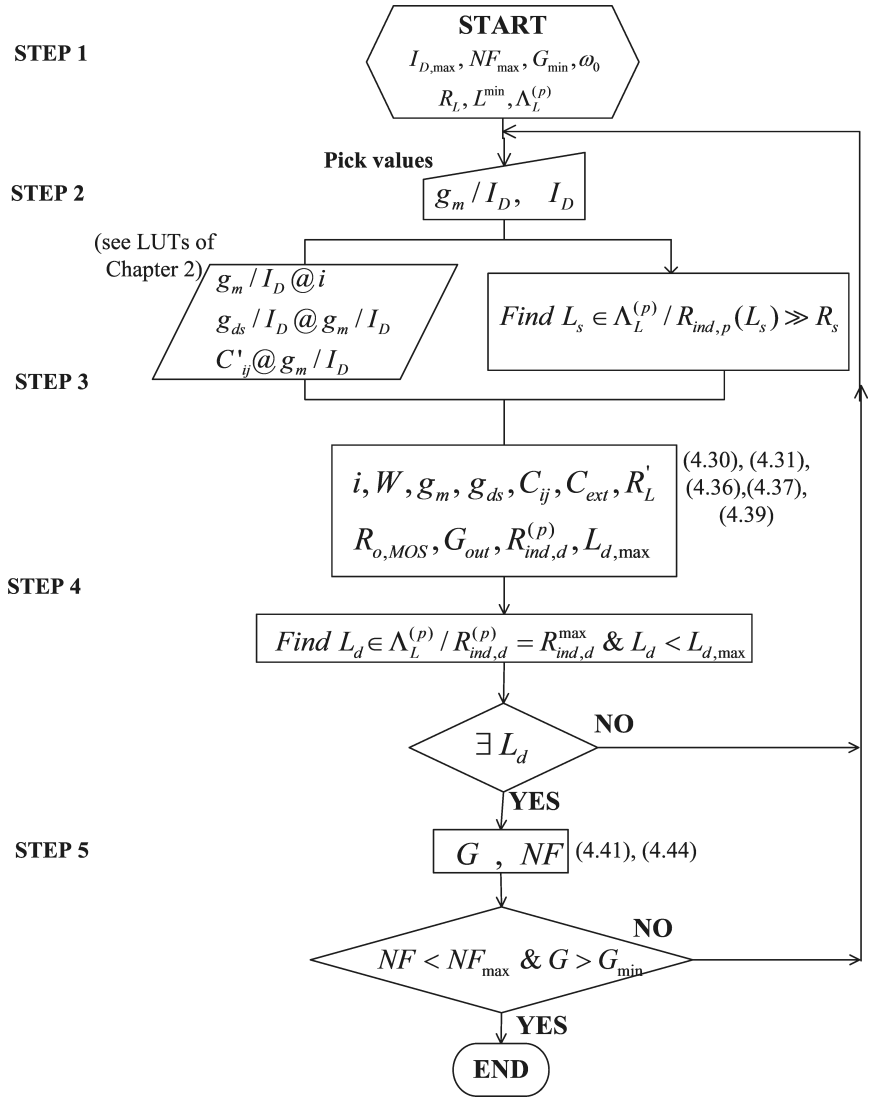


Figure 4.17: *Design flow of the CG-LNA architecture.*

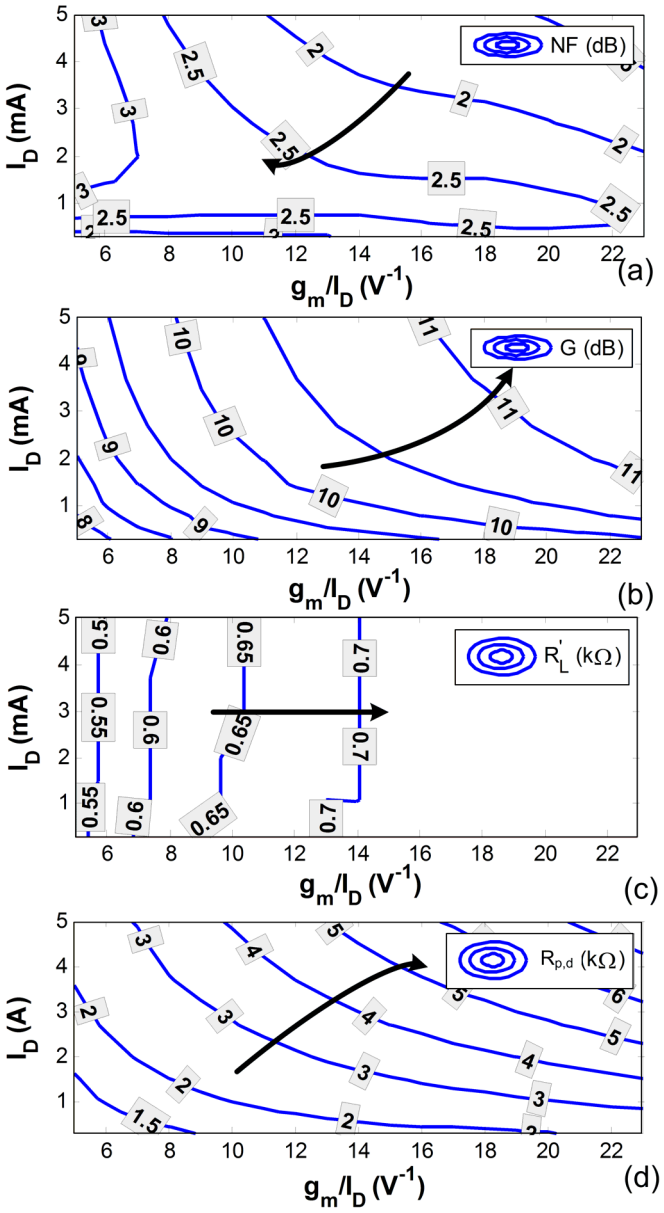


Figure 4.18: *(a) Noise figure (b) Power gain, (c) $R_L^{'}$ and (d) $R_{p,d}$ versus I_D and g_m/I_D.*

the noise figure increases when moving to moderate and strong inversion, due to the increment in the drain noise term of (4.42).

The power gain is plotted in Fig. 4.18.(b), which it is observed an increasing tendency in the direction of the arrow; the power gain increases when moving to weak inversion and when the bias current raises.

The behavior of resistor $R_L^{'}$ is depicted in Fig. 4.18.(c); it is almost independent of I_D and increases when moving to weak inversion. A limit around 720 Ω exists due to the maximum transistor width reachable. Moreover, the maps of $R_{p,d}$ are presented in Fig. 4.18.(d); this resistance increases with the bias current and when moving to weak inversion.

4.3 Conclusions

This chapter presents the third and four steps of our RF design methodology (exposed in Chapter 1) for two topologies: CS-LNA and CG-LNA, for RF nanometer technologies based on the g_m/I_D technique. The proposed methodology enables a considerable design time reduction as little re-design is needed. It also shows the design compromises of the LNAs, providing beforehand a complete panorama of the LNA behavior when bias and inversion level is modified.

The study of the CS-LNA design space has been done by covering acceptable current values and the MOS transistor parameter g_m/I_D, in order to study the trade-offs of using different MOS transistor inversion levels in the design. Both MOST and inductor data were extracted with SpectreRF simulations to accurately and quickly model these components and include the database in the design flow. The inclusion of the flicker noise in the noise figure computations is proven to be needed in moderate and strong inversion zones. R_{bias} is added in the gain and noise figure computation and it is shown their degradation when R_{bias} decreases. The maps of noise figure, power gain, C_t and L_s versus the pair (g_m/I_D, I_D) were displayed to see their behavior as the inversion level and bias current change. It has been highlighted how designing in moderate inversion leads to a good compromise of power reduction and acceptable noise figure and gain levels. Two application examples were implemented as a demonstrator of the presented method. Noise figure and gain values obtained from mathematical computations following the method, electrical simulations and measurements accord with each other with acceptable error levels.

Finally, the architecture study and the design flow of the CG-LNA considering real inductors is presented, to cover other LNA architectures in which the design methodology presented in Chapter 1 can be applied.

4.A Appendix A: CS-LNA $Z_{o,MOS}$ expression

The output impedance of the CS-LNA Core Stage directly depends on the load seen from the source of M_2 to ground, which we call Z_{S2}. This load includes the effect of R_s, L_g, C_{ext}, and M_1 transistor transconductance g_m, g_{ds}, C_{gs} and C_{gd}. As in the rest of the work, M_1 is considered identical to M_2. The small-signal schematic of Fig. 4.19 is used to obtain $Z_{o,MOS}$. For this study, capacitor C_{gd} has been considered as its feedback changes the output impedance, especially for MOST with large widths.

To compute Z_{S2}, it is considered two impedances: 1) Z_{G1}, the impedance seen from the gate of M_1 to the input (which is grounded); and 2) Z_{vin}, the impedance seen from the gate of M_1. Then, Z_{G1} is

$$Z_{G1} = (R_g + R_s) + sL_g, \tag{4.45}$$

and Z_{vin} is

$$Z_{vin} = \frac{v_{g1}}{i_t} \approx sL_s + \frac{1}{sC_t} + L_s\frac{g_m}{C_t}. \tag{4.46}$$

From these equations, Z_{S2} is

$$Z_{S2} \approx \frac{\frac{1}{sC_{gd}} + \frac{Z_{vin}Z_{G1}}{Z_{vin}+Z_{G1}}}{1 + \frac{g_m Z_{G1}}{sC_t(Z_{vin}+Z_{G1})}} \tag{4.47}$$

Then $Z_{o,MOS}$ has the following expression

$$Z_{o,MOS} \approx \frac{1 + (g_m + sC_{gs})Z_{S2}}{g_{ds} + sC_{gd}(1 + (g_m + sC_{gs})Z_{S2})}. \tag{4.48}$$

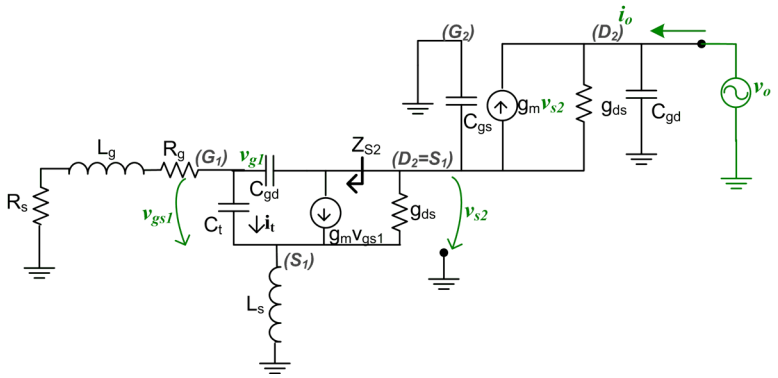


Figure 4.19: *Schematic used to calculate CS-LNA $Z_{o,MOS}$.*

CHAPTER 5

Design Methodology Applications in a Complex System

THE IMPLEMENTATION OF a low-power 2.4-GHz ZigBee transceiver is one of the goals of the main project in which this thesis has been embedded. To reach this objective, intermediate steps were performed to test the possible architectures of the involved blocks. This chapter presents the implementations of some RF preliminary blocks where our developed design methodology (or part of it) has been used. It also introduces the final ZigBee transceiver analog front-end.

The list of circuits begins with the implementation of a single-ended-input RF receiver front-end, presented in [Fior 11c]. With this block we aimed to check the pros and cons of using a single-ended input instead of a differential one. This front-end utilizes a single-ended CS-LNA, designed under the design methodology studied in Chapter 4. We deduce the front-end and CS-LNA specifications from the ZigBee requirements presented in [Vill 07]. The same CS-LNA was fabricated as a separate block in order to test it individually. Section 5.1 introduces the implemented circuits as well as their simulation and measurement results

The referred project also includes the study and design of built-in self-test (BIST) of RF circuits. We use a modified version of the previous single-ended CS-LNA to implement a demonstrator of a BIST technique using an on-chip envelope detector, which we present in [Barr 11a, Barr 11b] and we describe in Section 5.2. This dissertation only provides a brief discussion concerning the adjustments done in the LNA as well as the measurements of the on-chip demonstrator.

The transmitter front-end of the ZigBee transceiver needs a power amplifier (PA) to deliver the required power to the antenna. We designed a Class C PA, based on the design methodology we presented together with Barabino in [Bara 10]. That methodology considers the characterization techniques of MOST and passive components presented in Chapter 2, using them for describing a large-signal circuit behavior. In Section 5.3 PA measurements are provided.

Finally, an overview of the design of the ZigBee transceiver analog front-end is introduced in Section 5.4. For this design two new LNA and PA circuits with new specifications were designed, reflecting the fact of the reduction in the design time from specifications to layout, once computational routines are developed.

5.1 Single-ended input 2.4-GHz ZigBee receiver front-end

To study the feasibility of utilizing a single-ended input LNA in the ZigBee receiver, it has been designed a single-ended input differential-output RF front-end, which was presented in [Fior 11c]. It consists of a single-ended CS-LNA, AC coupled to a differential switched transconductor mixer (SW-MIX) [Klum 04], which schematic is shown in Fig. 5.1. We consider the possible use of a single-ended LNA since it enables 1) discarding the use of an input balun or a differential antenna, 2) reducing to half the power consumption of the block as there is only one LNA branch, and 3) reducing the silicon area. However, the second order intermodulation increases respect to a differential LNA. For our design, acceptable results in terms of linearity are observed, as the IIP2 exceeds the 10.5 dBm [Oh 05] which are expected in a ZigBee receiver. As the whole receiver was planned to work under a low-IF scheme, we implemented this structure accordingly. The used intermediate frequency was 2.5 MHz, to reduce the flicker noise effects and to achieve a good trade-off with the specifications of the baseband circuits at the receiver back-end as well as to simplify the PLL frequency division since an integer divider is required. The LNA has two-gain modes: high gain mode (hg) is used when low signal levels arrive to the system; low gain mode (lg) is applied when high input signals at the mixer input can cause signal compression due to the mixer non-linearities.

As the structure was used to evaluate the single-ended alternative, we discarded the use of packaging for test. Instead the front-end has been designed to be tested with microprobes. The LNA and the mixer were designed separately to be tested individually. As all the RF equipment of our laboratory is single-ended and has 50 Ω-input impedance, the single-ended input of the CS-LNA and each of the LO inputs of the SW-MIX (where the external clock is injected) as well as the output of the CS-LNA and the inputs of the SW-MIX were all matched to 50 Ω, as Fig. 5.1.(b) depicts. At the output of the SW-MIX, an external buffer is placed to enable the 50-Ω input impedances of the Spectrum Analyzer or the Noise Figure Analyzer connectors.

LNA and mixer were biased to work in moderate-weak inversion region in order to minimize the power consumption and also to enable the possibility of reducing the supply voltage, especially due to differential transconductor mixer architecture used.

The ZigBee receiver, and hence, the front-end, were specified to work in the 2.4 GHz-2.5 GHz band with a supply voltage of 1.2 V. The specifications of voltage conversion gain CG_V, noise figure NF, IIP3 and P1dB are listed in Table 5.1. These data are obtained by considering the ZigBee standard requirements and the other chain blocks of the receiver as presented in [Vill 07]. The noise figure specification

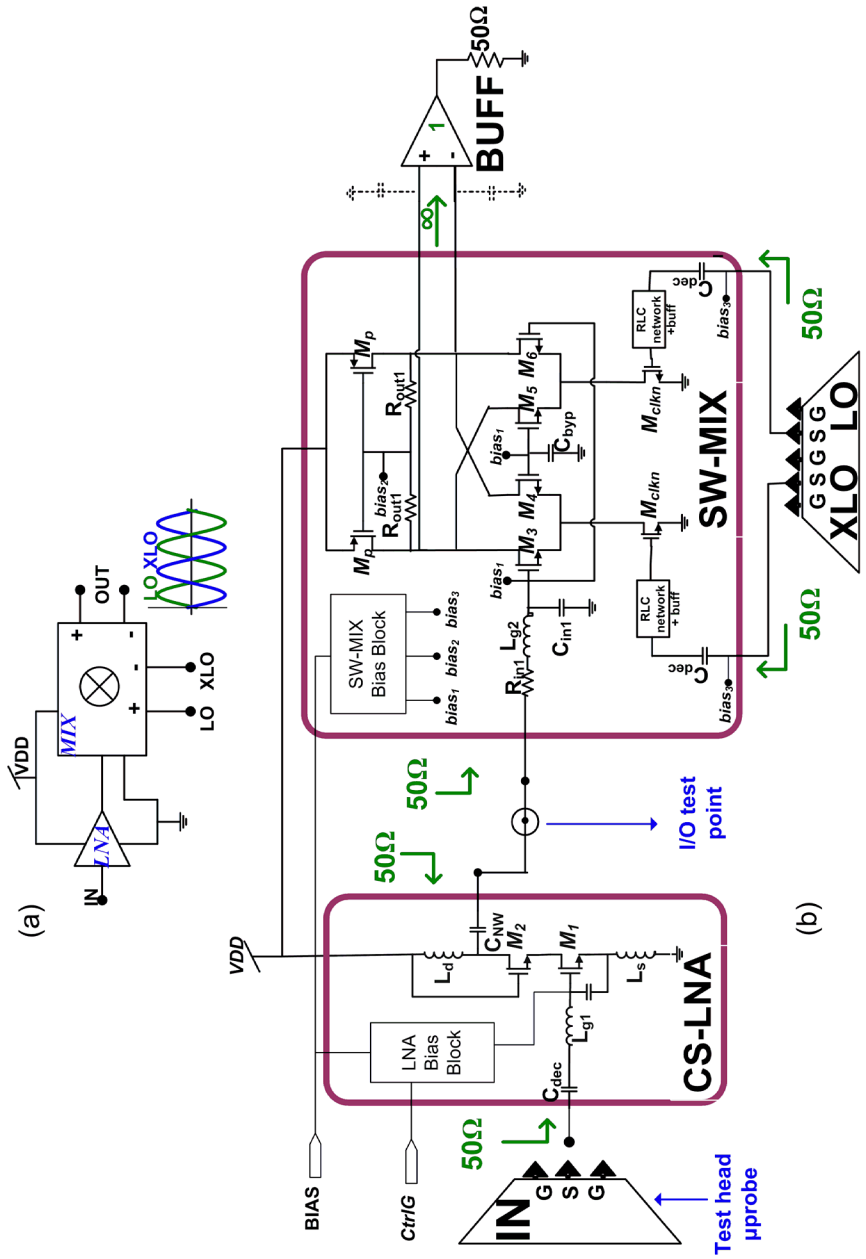


Figure 5.1: *(a)Front-end general scheme and (b) front-end scheme with the CS-LNA and SW-MIX schematics*

Parameter	Total Front-End	CS-LNA	SW-MIX
CG_V (dB)	>25	>10	>15
NF_{hg} (dB)	<12	<5	<15
$P1dB_{lg}$ (dBm)	>-23	>-10	>-15
$IIP3_{lg}$ (dBm)	>-13	>0	>-5

Table 5.1: *Front-end specifications.*

is given for the *hg* mode of the LNA, since in this mode the input signals are lower and are more affected by the intrinsic noise of the device. The opposite situation happens with the 1dB compression point, P1dB, and the IIP3 characteristics, which are specified for *lg* mode, since the system is more demanded in terms of linearity when high input signals arrive, and hence, when the LNA is set to *lg* mode.

The LNA design will be detailed in next section (Section 5.1.1). The SW-MIXER has been designed by other member of the research group, so it is not part of this thesis and hence it is not discussed here. Only for presenting a general panorama, the specifications of the mixer and its achieved features are listed in Table. 5.2. A complete discussion of this design can be found in the works of [Vill 10] and [Fior 11c].

The front-end final layout is presented in Fig. 5.2; it has an area of 0.74 mm^2, which 45% of this area is ocupied by the SW-MIX. As two-third of the mixer area is occupied by the matching network inductors of the LO ports and of one of the input matching network inductor -whose input is grounded-, the effective area of the front-end is 0.52 mm^2.

Table 5.3 presents the post-layout simulated results and the measurements of the fabricated front-end. The results of the post-layout simulations cover the specifications of Table. 5.1. We provide the NF for 2.5 MHz and 10 MHz because our specific equipment for noise figure measurements, the Agilent E4440A Spectrum

Parameter	CS-LNA Specs.	CS-LNA Post-layout	SW-MIX Specs	SW-MIX Post-layout
CG_V (dB)	>10	12.4/9	>15	20
NF_{hg} (dB)	<5	3.7 (hg)	<17	15.1
$IIP3_{lg}$ (dBm)	>0	-1.2	>-5	-3.5
P(mW)	lowest	1.44/0.92[a]	lowest	3.24/5.9[b]

[a] *hg/lg* modes

[b] Inferred from the total measured current of 6.9/6.47 mA (hg/lg) minus the simulated current of 3.0 mA of the first level clock buffers.

Table 5.2: *CS-LNA and SW-MIX specifications and post-layout simulations.*

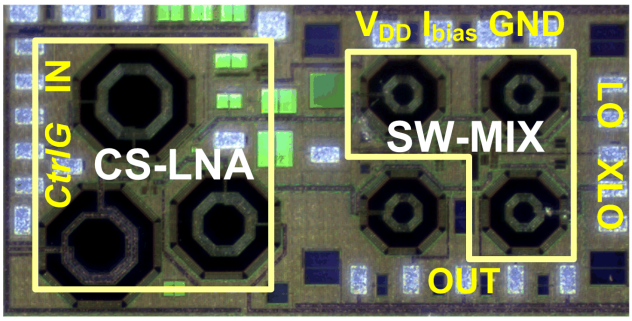


Figure 5.2: *Front-end microphotograph.*

Analyzer, only reaches frequencies down to 10 MHz; for frequencies lower than 10 MHz the NF measurements were made with the Agilent N8974A Noise Figure Analyzer. The conversion gain was measured with the Spectrum Analyzer in the 0.5 MHz-16 MHz band. Post-layout simulated results and measurements of the NF and *CG* are presented in Fig. 5.3.(a) and (b). Differences in the *CG* are expected since the model of the mixer load is not very accurate.

Finally the in-band test of IIP3, measured with two-tone input signal, $f_{RF_{1,2}} = f_{LO} \pm f_{IF} \pm 0.3MHz$, with f_{LO}=2.445 GHz and f_{IF}=2.5 MHz, is shown in Fig. 5.4.(a), with an extrapolated IIP3 of -12.8 dBm. The P1dB in *hg* mode is around -26 dBm, then, giving a security margin of 4 dB, we infer that the *hg* mode should be used up to -30 dBm. Above it and up to -20 dBm, the LNA should switch to *lg* mode. Fig. 5.4.(b) presents the output spectrum for a -35 dBm OQPSK input signal.

With the FoM of [ITRS 09] (see (4.28)), a list of active front-end circuits is presented in Table 5.4. Very good results are obtained, especially compared with the most recently reported, as [Nguy 10, Zito 09]. The work of Liscidini, [Lisc 05],

Table 5.3: *Front-end post-layout simulations and measurements.*

Parameter	Post-layout Sim.	Measurement
Current (hg/lg) (mA)	3.9/3.47	3.9/3.47
CG_V @ 2.5MHz (hg/lg) (dB)	32.5/30	30/28
NF @ 2.5MHz (hg) (dB)	8.5	7.5
NF @ 2.5MHz (lg) (dB)	9.3	9.6
IIP3 (hg) (dBm)	-12.8	-16.2 $\pm$ 1.0
IIP3 (lg) (dBm)	-9.8	-12.8 $\pm$ 1.5
IIP2 (hg) (dBm)	-	14.4 $\pm$ 1.0
Zin @ 2.445GHz (Ω)	44.7	47
S11 of In port @ 2.445GHz (dB)	-24	-21

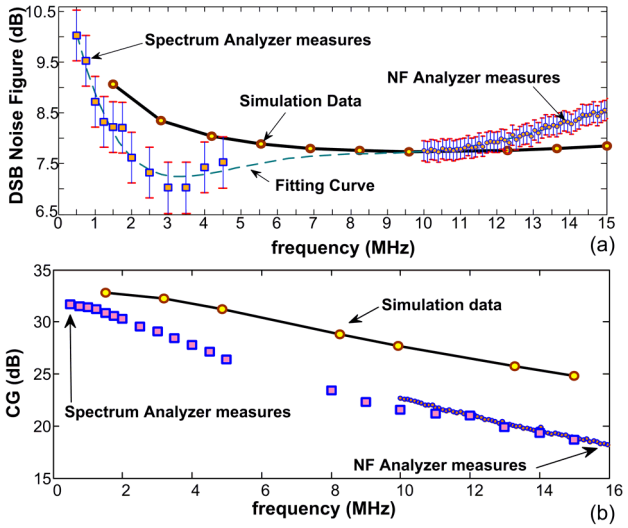


Figure 5.3: *Comparison of measured versus simulated (a) NF and (b) CG of the front-end (hg case) for a -35dBm input.*

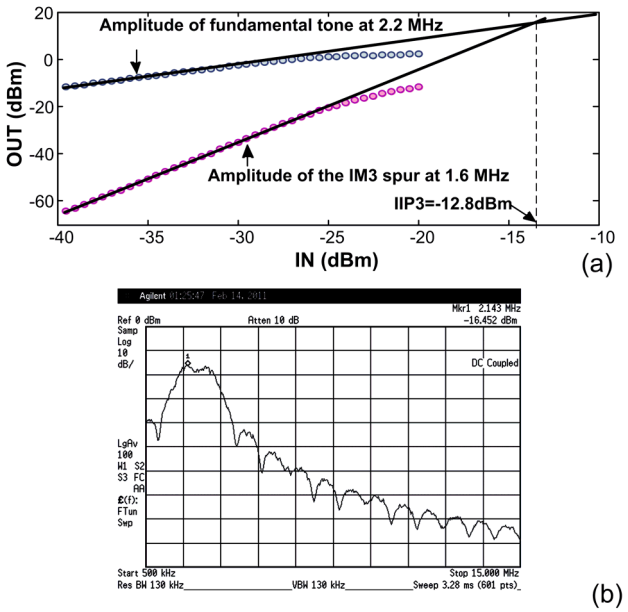


Figure 5.4: *(a) Measured IIP3 for the low gain case and (b) front-end output spectrum of a -35dBm OQPSK input signal.*

has better FoM due to its low noise figure, but its very high power consumption is not very suitable for ZigBee applications.

As conclusions, a single-ended input front-end for low power, suitable for ZigBee has been designed. The use of a single ended input CS-LNA reduces power, area and external chip components. The operation of MOS transistor in moderate and weak inversion regions helps to reduce power and supply voltage. Finally good FoM has been achieved compared with other ZigBee front-ends designs. The linearity of the block is acceptable for a ZigBee receiver.

Table 5.4: *Comparison between the designed front-end (F-E) and other published works.*

Ref.	**tech.**	**CG(dB)**	**NF(dB)**	**IIP3(dBm)**	**Power(mW)**	f_0**(GHz)**	**FoM(MHz)**	**Obs.**
F-E$_{lg}$	90nm	28	9.6	-12.8	4.68	2.445	95.4	-
F-E$_{hg}$	90nm	30	7.5	-16.2	4.68	2.445	85.7	IIP2=14.4dBm
[Nguy 10]	180nm	22	9	-15	5.4	2.445	25.9	dual band
[Zito 09]	SiGe350nm	26	8.7	-13	8.6	2.445	44.3	-
[Song 06]	180nm	31.5	11.8	NA	0.5	2.4	-	NF @ 10MHz
[Jarv 05]	130nm	14.5	24.5	-21	1.68	2.445	0.2	out-of-band IIP3
[Kwon 05]	180nm	19	11	-9	4.25	2.445	55.7	IF=480 MHz
[Lisc 05]	130nm	23.4	5.8	-4.8	24	2.3	167.5	802.11b-g
[Beff 02]	180nm	21.4	13.9	-10	6.48	2.445	18.8	IF=2 MHz

5.1.1 Single-ended CS-LNA design

The single-ended CS-LNA of the front-end previously described was implemented in a stand-alone version to verify the proposed methodology and to demonstrate a BIST stragegy for RF blocks, which will be described in Section 5.2.

The implemented CS-LNA schematic is seen in Fig. 5.1.(b). We follow the LNA design methodology presented in Chapter 4 to obtain this LNA design. In this chip, the silicon area was a strong constraint, so the maximum value of the MOS transistor bias resistance, R_{bias}, (already presented in Chapter 4) was limited again to 1 kΩ, in the same way as happened with the differential CS-LNA design of Section 4.1.5. Table. 5.5 presents the results of the computed design (under nominal conditions, with *hg* mode), the simulated schematic and the layout simulations. In *lg* mode, the current drops down to 0.8 mA, the post-layout gain moves to 9 dB and the IIP3 raises to -1.24 dB, consuming 0.92 mW, while in *hg* mode it increases up to 1.44 mW for a 1.2 V power supply.

The microphotograph of the single-ended LNA is shown in Fig. 5.9.(a), where all the components and blocks are highlighted.

LNA measured S-parameter are shown in Fig. 5.5. The frequency range of the measurements includes the ZigBee band of 2.4 GHz-2.5 GHz. The measurement set-up is the same as the one used for the differential CS-LNA of Section 4.1.5. The input network is centered at 2.42 GHz, in the band of interest ($|S_{11}| \leq -20$ dB). The output network resonant frequency has a shift of 150 MHz down, visualized when trace $|S_{22}|$ minimizes at 2.3 GHz ($|S_{22}| < -20$ dB), which again affects the gain and the NF responses, shift down their maximums and minimums. It also has

Characteristics		Calc.	Sim.	Post-layout
I_D (mA)		1.2	1.2	1.21
g_m/I_D (V^{-1})		17	17	17
L_s (nH)		0.8	0.8	1.1
L_g (nH)		7.9	7.9	9.8
L_d (nH)		9.4	7.1	7.1
W_{M_1} (μm)		165	165	157
C_{gs} (fF)		158	150	151
C_{ext} (fF)		207	200	141
G (dB)	R_{bias}=10kΩ	15.4	14.5	-
	R_{bias}=1kΩ	14.4	13.0	12.5
NF (dB)	R_{bias}=10kΩ	1.9	2.3	-
	R_{bias}=1kΩ	3.0	3.6	3.7
IIP3 (dBm)		-	-5.2	-4.4

Table 5.5: *Single-ended CS-LNA component values comparison between Matlab and Spectre RF simulations.*

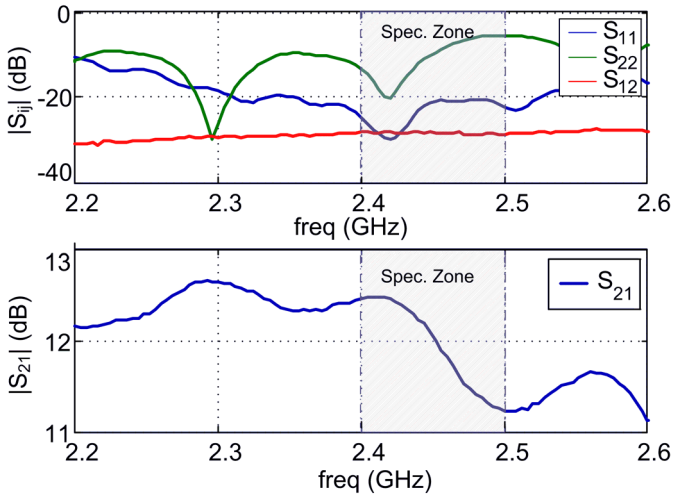


Figure 5.5: *Single-ended CS-LNA measured scattering parameters at hg mode.*

a notch at 2.42 GHz, which is a consequence of a minimum in $|S_{11}|$. For the *hg* gain mode, we have a maximum in $|S_{21}|$ of 12.65 dB at 2.3GHz and, as expected, another peak of 12.5 dB at 2.42 GHz. At the designed frequency of 2.445 GHz the gain is 12.2 dB, which is very near the gain value obtained by post-layout simulation. The gain isolation is around -30dB.

Noise figure is plotted in Fig. 5.6, in the band of 2.2 GHz-2.6 GHz. A minimum zone is found in 2.3 GHz, with a NF of 4.2 dB. For the design frequency of 2.445 GHz, the NF reaches 4.3 dB. Those values are 0.6 dB above the post-layout datum, which is an acceptable difference between measurement and simulation.

IIP3 and IIP2 values were obtained using two-tone input signals. Frequencies of f_{01}=2.446 GHz and f_{02}=2.4465 GHz have been used for the in-band IIP3 test,

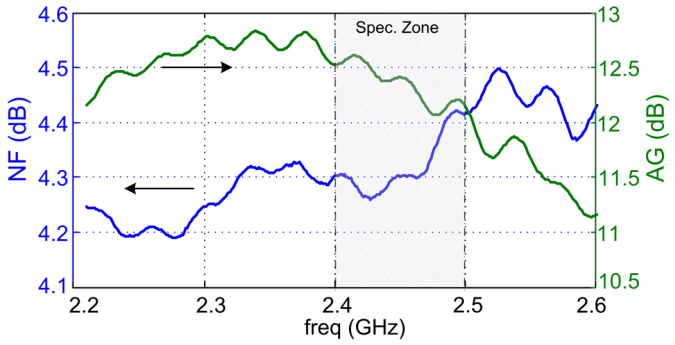


Figure 5.6: *Single-ended CS-LNA measured NF and available gain AG at hg mode.*

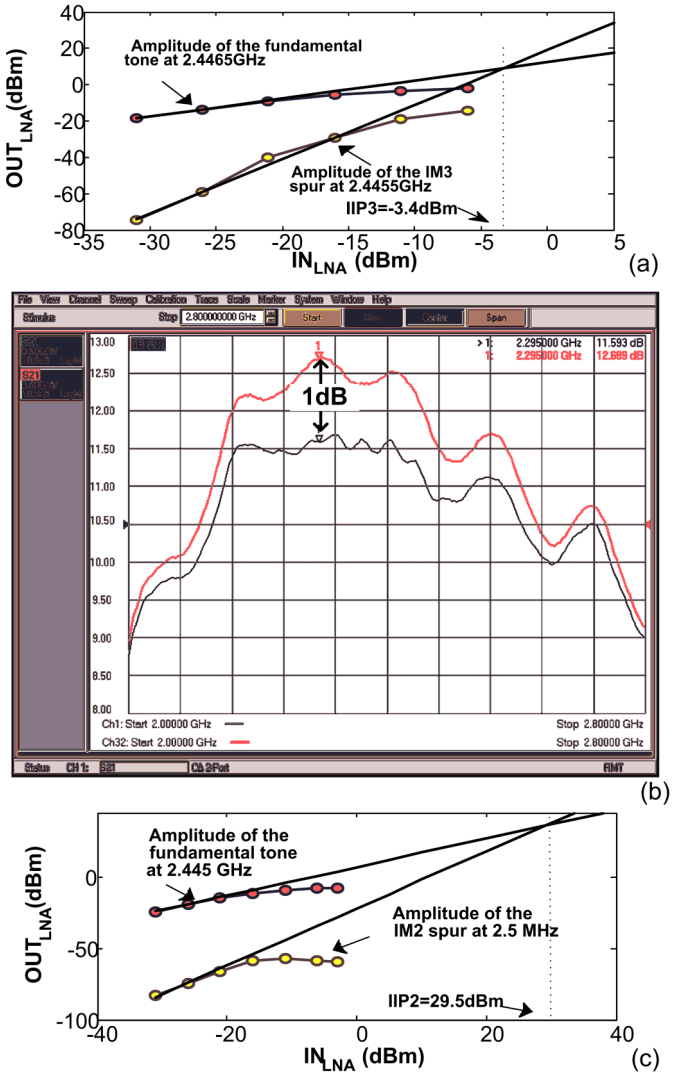


Figure 5.7: *Measured (a) IIP3, (b) P1dB and (c) IIP2 of the single-ended LNA at hg mode.*

with a measured output frequency of 2.4455 GHz. As Fig. 5.7.(a) stands, the measured IIP3 is -3.4 dBm for the *hg* mode. We also measure the 1dB compression point P1dB, with the network analyzer, as seen in Fig. 5.7.(b); the gain falls 1 dB when the input power is -11.5 dBm. The IIP2 measurement data are shown in Fig. 5.7.(c). Similarly, an IIP2 two-tone test with frequencies of f_{01}=2.445 GHz and f_{02}=2.445 GHz+2.5 MHz, have been used; doing the intermodulation, the spur falls in the 2.5 MHz IF band. The measured value was 29.5 dBm, a very good value considering the single-ended architecture and the lack of internal calibration.

5.2 Demonstrator for an RF BIST methodology

This section presents the RF Built-in Self Test (BIST) demonstrator which validates the methodology for testing embedded LNA we presented in [Barr 11a]. It is based on the detection and analysis of the response envelope to a two-tone input signals of an RF block, e.g. an LNA. The description of this methodology, out of the scope of this work, is fully discussed in [Barr 11a] where we showed the feasibility of coupling the envelope detector to an LNA output. A slightly modified version of the LNA included in the receiver front-end exposed in Section 5.1.1 has been used as a part of this demonstrator, just adjusting the LNA output network to match the whole design to 50 Ω. The schematic is visualized in Fig. 5.8. The layout is depicted in Fig. 5.9. We have used the envelope detector architecture presented in [Cha 09], which comprises a voltage-to-current converter and an AC-coupled half-wave current-mode rectifier with a passive low-pass filter.

The simulated results of the CS-LNA characteristics with and without the envelope detector and the measurements are listed in Table 5.6. No appreciable variations are observed among the simulated characteristics of the block with and without the envelope detector. For the measured results, the NF differs from the simulated characteristics in 0.5 dB, which is an acceptable spread for noise figure measurements. The measured input waveform of the envelope detector (output of the CS-LNA) and output of the envelope detector, obtained with the Oscilloscope DSO81304B Infiniium of Agilent, are presented in Fig. 5.10. As it is expected, the output signal follows the envelope of the input signal.

This single-ended CS-LNA has also been used as a demonstrator of the RF alternate test using multi-VDD conditions method we presented in [Barr 11b].

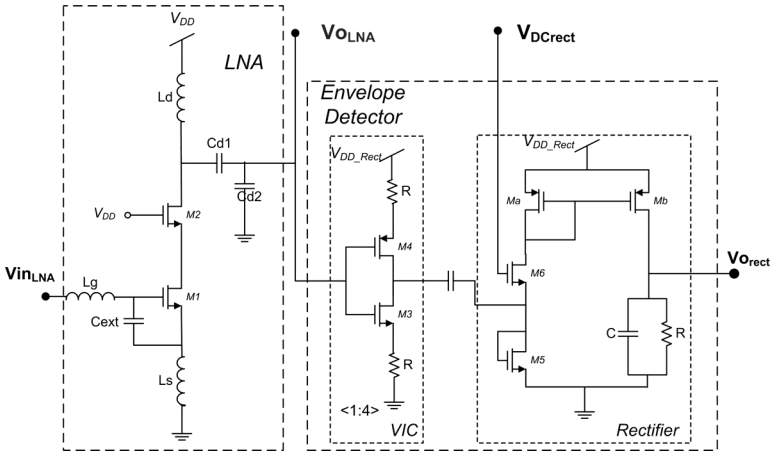


Figure 5.8: *Schematic of the CS-LNA with the envelope detector.*

Table 5.6: *CS-LNA characteristics measured and simulated with and without envelope detector.*

Specification	LNA without envelope detector	LNA with codesigned envelope detector	Measured with envelope detector
Gain (dB)	12.5	12.4	12.3
NF (dB)	3.66	3.66	4.25
IIP3 (dBm)	-4.4	-3.5	-4
CP1dB (dBm)	-15	-15.1	-12.5
S_{11} (dB)	-24.8	-25.2	-21.1
S_{22} (dB)	-9.8	-11.3	-11.2
S_{12} (dB)	-26.4	-26.5	-28.2

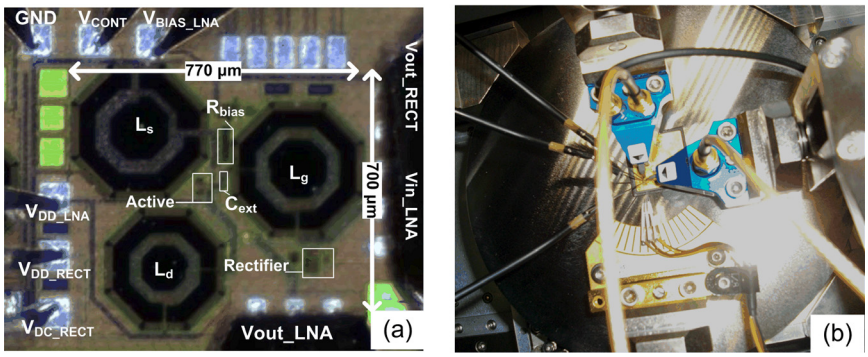


Figure 5.9: *(a) Microphotograph of the single-ended CS-LNA with the Envelope Detector where active area and passive components are highlighted. (b) Single-ended CS-LNA with the Envelope Detector measurement set-up.*

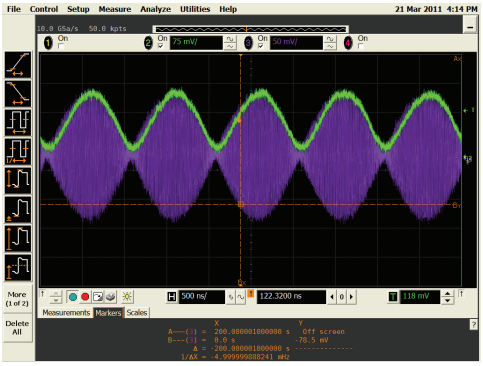


Figure 5.10: *Measured input signal of the envelope detector (in magenta) and output of the envelope detector (in green).*

5.3 Class-C PA design

The ZigBee transceiver needs a power amplifier (PA) that provides the required power to the antenna. We have designed a PA [Fior 10] following the Classes A-AB-C PA design methodology we presented in [Bara 10]. In this methodology we apply similar ideas the one presented in the general design methodology of Chapter 1, but in a large-signal design. In this method: 1) the DC behavior MOS transistor and the passive component are equally modeled, 2) the PA is described by means of a set of large-signal expressions and 4) a design flow, which uses items 1), 2) and 3) is developed. The PA described in this section reasserts the validity of working with semi-empirical device models in RF circuits. Furthermore, as presented in [Bara 10], it shows that this validity is extended to a design with the MOS transistor operating in a non-linear large-signal mode as it is the case of Class C PAs.

As Class C PAs supports phase modulations they can be used in a ZigBee implementation. A differential topology was designed and fabricated, despite the method is developed for a single-ended scheme. The PA was implemented in the TECH1 technology, having all the inductors on-chip. The scheme used is presented in Fig. 5.11, where the differential source and load impedances are real and equal to 100 Ω. The PA consists of an active block (MOS transistor M_1) and an output network (L_{out}, C_{out1}, C_{out2} and R_{bias}); the input network is used to couple the input signal (coming from a 50 Ω RF signal generator) to the gate of the transistor M_1, the effective PA input.

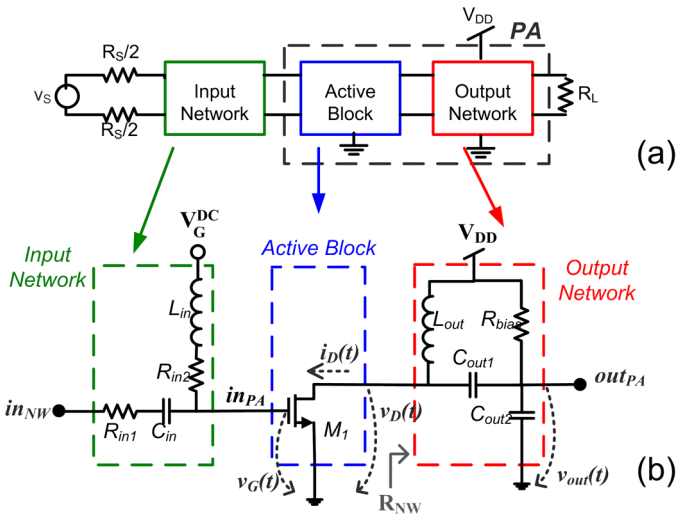


Figure 5.11: *Schematic of the designed PA: (a) differential scheme (b) single ended view.*

The PA design flow sets a group of PA specifications (output power of the fundamental tone P_{out}, second and third harmonic output power, $P_{harm}^{2^{nd}}$ and $P_{harm}^{3^{rd}}$ and power efficiency η) and fixes two boundary conditions: 1) to give the maximum power to R_L, the maximum voltage swing at the drain voltage must be fixed to $[0, 2V_{DD}]$, and 2) the MOS transistor minimum length L_{min} to reach high f_T. With the specifications and the boundary conditions, the design flow of [Bara 10] is applied, obtaining a final design where the transistor width, the output network sizing, the DC gate voltage v_G^{DC} and the maximum amplitude at the gate v_G^{RF} are set.

The PA design flow of [Bara 10] is briefly resumed below. To implement it, the data of Chapter 2 is previously needed: 1) MOS transistor LUTs, and 2) inductors LUT. The design flow is:

Step 1) Due to filtering of the output network: 1) the voltage signal at the drain of M_1 is almost sinusoidal and the peak value is almost V_{DD} (if the DC drain voltage is fixed to V_{DD} and 2) the load resistance R_L is transformed to a resistance seen from the drain, R_{NW}. Then, calculate $R_{NW} \cong 1/2V_{DD}^2/P_{out}$.

Step 2) Choose a pair of values for the DC gate voltage and the RF peak gate voltage, which sum does not surpass V_{DD} and subtraction is above zero.

Step 3) The two main hypothesis of [Bara 10] are: 1) the normalized drain current in each time interval, for a whole period, is obtained by using the normalized current i, considering that the gate and drain voltages of the MOS transistor LUT are the instantaneous gate and drain voltages, (considering no difference of phase between the instantaneous drain and gate voltages; and 2) the MOST is working under the quasi-static condition.

With these hypothesis, find the normalized drain current in the time domain, as well as its DC, fundamental, second and third harmonic ($\widehat{I_{DC}}$, $\widehat{I}_1$, $\widehat{I}_2$, $\widehat{I}_3$), applying Fourier expansion.

Step 4) Calculate the MOS transistor efficiency η_{MOS} with $\eta_{MOS} \cong \widehat{I}_1/2\widehat{I}_{DC}$.

Step 5) Calculate the output network efficiency η_{NW} with $\eta_{NW} = 1 - R_{NW}/R_{p,ind}$, being $R_{p,ind}$ the parasitic resistance of the inductor. Calculate the total power efficiency of the PA as $\eta = \eta_{MOS}\eta_{NW}$.

Step 6) Calculate the MOST aspect ratio as $W/L = 2P_{NW}/(V_{DD}\widehat{I}_1)$, being P_{NW} the delivered power to the network, calculated as $P_{NW} = I_1 V_{DD}/2 = V_{DD}^2/(2R_{NW})$.

This methodology has been implemented in a set of MATLAB computational routines by Barabino. It generates maps of efficiency, transistor width and output inductor versus the pair of DC gate and signal gate voltages. The efficiency map is shown in Fig. 5.12.

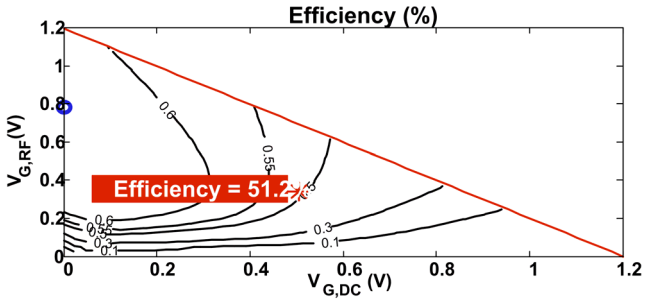


Figure 5.12: *Efficiency contours versus DC gate and signal gate voltage pair (V_G^{DC},V_G^{RF}).*

5.3.1 PA implementation

With the design flow and the computational routines, we design in TECH1 a Class-C PA, suitable for 2.4 GHz ZigBee transmitters. A summary of specifications is provided in Table. 5.7. This PA uses 1.2 V MOS transistor, so the V_{DD} could reach up to 0.65 V. The final design point chosen is a DC gate voltage of 0.5 V and a gate peak voltage of 0.4 V and an efficiency of 51.2% as shown in Fig. 5.12. The transistor width is 42.2 μm and the output network is: L_{out}=5.64 nH, C_{out1}=1.57 pF and C_{out2}=0.69 pF. The post-layout simulation results of the implemented circuit is listed in Table 5.8. The microphotograph of the PA is visualized in Fig. 5.13.

$P_{out} \geq 0$ dBm	$R_L = 100\Omega$	$V_{DD} = 0.65V$
$V_D^{RF} = 0.6V$	$R_{p,ind} > 1k\Omega$	$P_{harm}^{2nd} \leq -40$ dBc
$P_{harm}^{3rd} \leq -20$ dBc	$\eta > 35\%$	OP1dB=-10 dBm

Table 5.7: *Summary of the chosen PA specifications.*

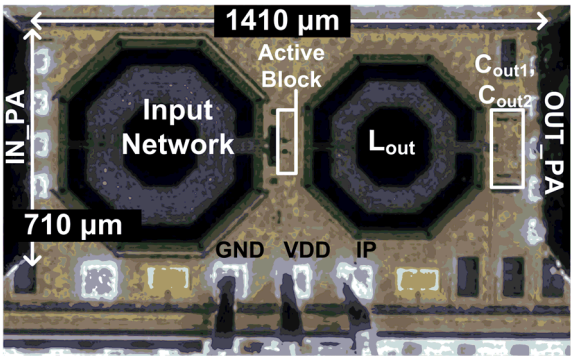


Figure 5.13: *Microphotograph of the designed PA*

Characteristics	Post-layout sims.	Characteristics	Post-layout sims.
V_{DD}	0.65 V	G_{pow}	26 dB
P_{DC}	3.16 mW	I_D	4.6 mA
η	46.6 %	$P_{harm}^{2^{nd}}$	-67 dBc
P_{out}	1.9 dBm	$P_{harm}^{3^{rd}}$	-21 dBc

Table 5.8: *PA characteristics of SpectreRF post-layout results for a input power at the input network of -2.5 dBm.*

The chip has been partially measured, and first results of differential efficiency and output power are presented in Figs. 5.14 and 5.15. The PA reaches efficiencies of 46% for input powers of -22 dBm. The 1 dB output power compression point OP1dB is -5dBm. The input power of the active block has been inferred from the 22.5dB of expected losses of the input network.

In Fig. 5.15.(b) a plot of the output power spectrum due to an input injected signal of -2.5 dBm and an inferred signal of -25 dBm at the input of the PA, is shown. The fundamental power was around -1 dBm (after cable loss corrections). The second harmonic has a value around -25 dBc and the third harmonic around -36 dBc. There is a variation in the second and third harmonics respect to the expected simulated values. It is due to the unbalanced output paths which cause this effect.

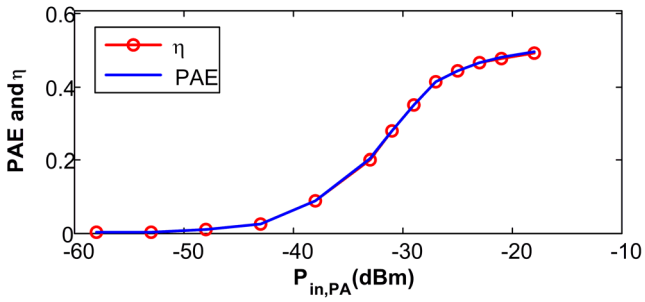


Figure 5.14: *Measured PA efficiency and power added efficiency PAE.*

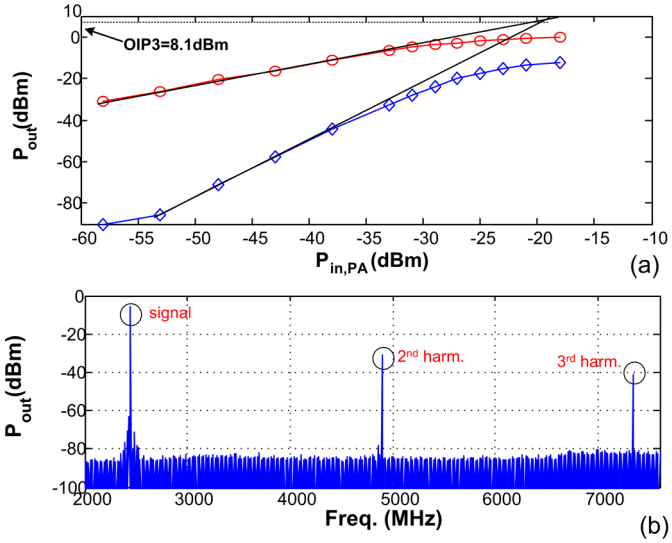


Figure 5.15: *(a)PA measured output power versus the inferred input power injected at the gate. (b) Measured output full spectrum of the PA for an input signal of -2.5dBm (no correction due to the set-up losses are applied).*

Finally the output spectrum of OQPSK with a signal bandwidth of 2 MHz is depicted in Fig. 5.16.

To conclude, a compatible IEEE 802.15.4 Class C PA design in 90nm CMOS is presented. It is based on the "Design efficiency approach" presented in [Bara 10]. Post layout results and preliminary measurements show very good agreement with MATLAB results. Preliminary measurement simulation results show similar results in term of efficiency and output power.

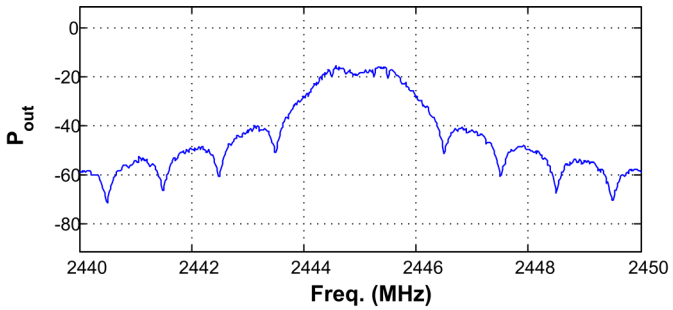


Figure 5.16: *PA output spectrum of an OQPSK modulated input signal (no correction due to the set-up losses are applied).*

5.4 Designed blocks in a ZigBee analog transceiver

This thesis work finished with the description of the design of a low-power 2.4-GHz ZigBee transceiver, which block diagram and microphotograph are shown in Fig. 5.17 and Fig. 5.18. We take part in the design of the LNA and the PA. In this ZigBee transceiver, a VCO was designed following a different approach that of resented in this thesis, by another designer of the group. The receiver and the transmitter architectures were fully-differential, so as the LNA and PA blocks. Due to lack of substrate models to emulate the amount of digital noise that reaches the RF blocks -generated principally by the PLL-, a differential scheme for all RF blocks was preferred to reject that noise, hence the single-ended LNA architecture already studied was discarded.

As the LNA and the PA for the analog transceiver were specified with a new set of values, two new designs for these blocks were done utilizing their already presented design methodologies. The designed LNA, at 2.445 GHz has a differential input impedance of 100 Ω and a differential output impedance of only 50 Ω, a voltage gain of 6 dB, a noise figure of 4.5 dB, an IIP3 of -7 dBm and a power consumption of 900 μA. The gain is lower than the differential design presented in Chapter 4 because the current is lower and the maximum L_d, and hence, the maximum $R_{ind,p}$ were lower due to the reduction in the single-ended load R_L from 50 Ω to 25 Ω.

The PA has been designed with 2.5 V-MOS transistors to use a V_{DD} of 1.2 V and to permit the MOS drain to have a maximum output excursion of 2.4 V. The M_1 transistor length is 280 nm (the minimum available for these MOS transistors) and its width is 104 μm. The final design point was: DC gate voltage V_G^{DC}=0.61 V and gate voltage amplitude V_G^{RF}=0.34 V, for each single-ended input. Its maximum DC power consumption is 3.7 mW, the output power reaches 2.5 dBm for a 100 Ω load, with an output P1dB of 0 dB, and an efficiency of 24 %. This fall in the efficiency of this PA respect to the one designed is due to the higher transistor lengh and the value of the maximum amplitude at its input, given by the up-conversion mixer.

Experimental results shown the correct operation of the receiver-transmitter system using two PCBs (Fig. 5.19), one with the chip acting as receiver and the other as transmitter. When an OQPSK baseband signal is injected at the transmitter baseband inputs, the output receiver signal after demodulation is shown in Fig. 5.20.(a) and the modulated OQPSK spectrum captured with the Spectrum Analyzer is presented in Fig. 5.20.(b).

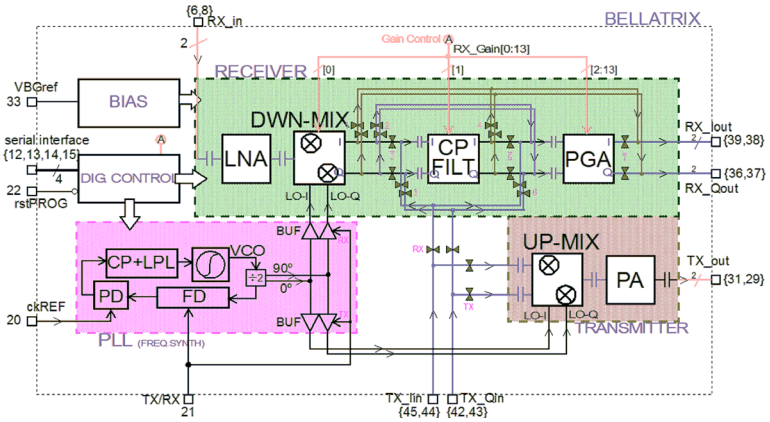


Figure 5.17: *Transceiver block diagram*

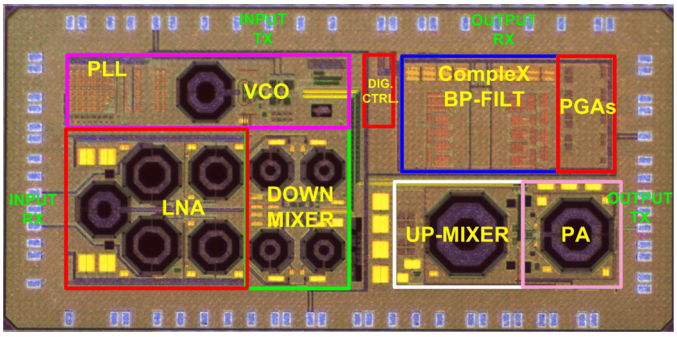


Figure 5.18: *Transceiver microphotography and sub-block and signaling distribution.*

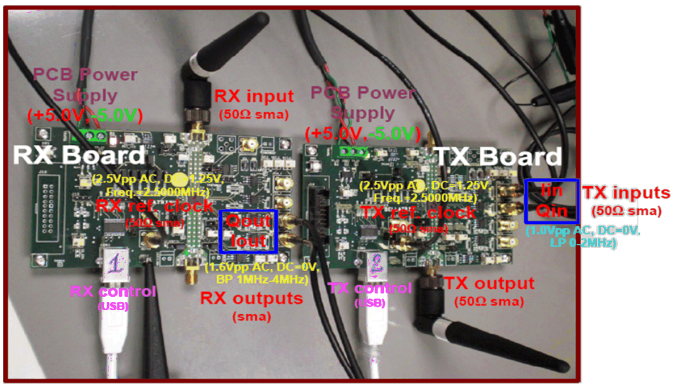
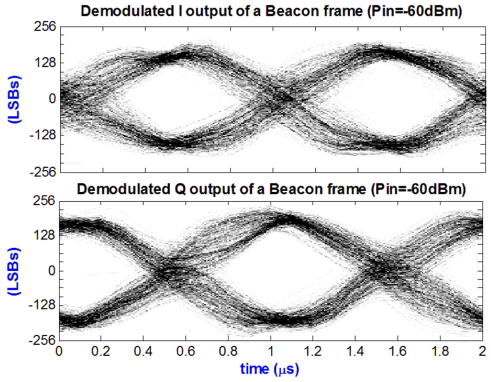
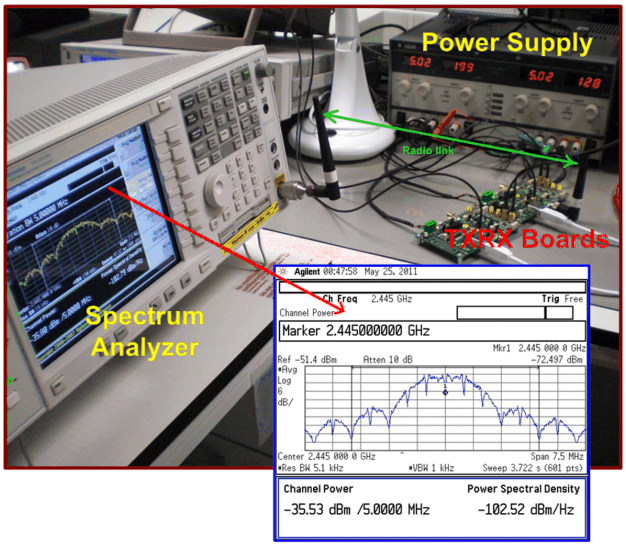


Figure 5.19: *Boards used in the transmission-reception experiment.*



(a)



(b)

Figure 5.20: *Transmission-reception experiment: (a) eye diagram of the demodulated receiver output of a ZigBee beacon frame and (b) transmission verification using a Spectrum analyzer, the inner image shows the modulated OQPSK spectrum.*

5.5 Conclusions

This chapter presents the final design of the complete analog ZigBee transceiver as well as the realization of a set of circuits implemented in previous stages. Only the overview of the final PA and LNA blocks implemented in the ZigBee transceiver was presented. All circuits designed followed the methodology of Chapter 1 or a modified version considering MOS transistor large-signal operation, as it is the case of the implemented PAs. Finally, the reuse of LNA and PA computational routines and technology LUT allow an effective reduction of design time.

CHAPTER 6

Conclusions and Future Lines

6.1 Thesis conclusions

- It has been developed a design methodology for analog radiofrequency blocks, focused to nanometer technologies and based on the transistor modeling in all-inversion regions.

- The design methodology easily presents the trade-offs involved in each particular design and the consequences of modifying the parameters of the RF block. It is noticed the reduction of design time when applying the methodology, as little adjustments are needed after the election of the design point, a fact proven in the designed circuits by electrical simulations and experimental implementation.

- It has been demonstrated the utility of the g_m/I_D tool in the RF design, by systematically covering all-inversion regions of the MOS transistor and by exploiting the MOS transistor potential and the performance trade-offs of the RF block.

- It has been validated the use of MOS transistor semi-empirical models based on the small-signal characteristics of the device: the transconductance over drain current ratio, g_m/I_D, versus the normalized current i, the conductance g_{ds}, the five capacitance of the quasistatic model and the noise parameters.

- The quasistatic limit of one tenth of the transition frequency, used to reduce the number of capacitances involved and to simplify the MOS transistor study, proves to be valid in the considered designs. Acceptable results are also obtained when working a bit beyond that limit.

- It has been proven the validity of RF passive devices simplified models, obtained by means of AC simulation at the working frequencies assumed.

- MOS transistor and passive devices modeling proves to be very efficient as the data is collected once and reutilized for all the circuits and design flows.

- It has been shown that for the implemented RF circuits, integrated in nanometer technologies, the best performance compromises generally occurs in the MOS transistor moderate inversion region. Good agreement exists between measurements on implemented designs and the values derived from the design flows.

- Specific design methodologies were derived for LNAs and LC-VCOs architectures.

  It has been considered the MOS transistor drain noise and flicker noise in all-inversion regions.

- In the LC-VCO, it has been studied the design compromises due to the inversion region and the tank inductor value. It is seen how designing in moderate/weak inversion leads to a consumption reduction and a phase noise increment; on the other hand reducing tank inductor values contributes to an improvement in the VCO spectral purity.

  It has been presented an LC-VCO phase noise model, based on the Hajimiri's model, for all-inversion region of the MOS transistor.

- The LNA performance study has been done varying the inversion level and the drain current of the MOS transistor. It is shown the good trade-offs obtained when working in moderate/weak inversion regions in terms of noise and gain.

  The LNA noise figure analytical expression has been expanded by including the MOS transistor flicker noise.

  A study of second order effects of the LNA input bias resistance has been developed.

6.2 Future lines

- Validate with fabricated circuits the CG-LNA methodology sketched at the end of Chapter 4.
- Use the methodology in complex circuits as two-stage LNAs or multi-stage PAs.
- Study the viability of using the design scheme for higher frequencies, including the MOST non-quasistatic effects, when needed.
- Include a model of the layout parasitics in the design methodology, as in the LNA case the performance is degraded when the schematic is translated to the layout.
- Utilize the final design obtained with computational routines that implement the design flows as starting points in automatic optimization tools.
- Intend to implement a MOS transistor semi-empirical model based on EKV or ACM analytical expressions.

CHAPTER 7

Conclusiones y Líneas Futuras

7.1 Conclusiones de la Tesis

- Se ha desarrollado una metodología de diseño para bloques analógicos de radiofrecuencia, enfocada a tecnologías nanométricas y basada en el modelo de transistor para todas las regiones de inversión.

- La metodología de diseño presenta fácilmente los compromisos involucrados en cada diseño en particular y las consecuencias de modificar los parámetros del bloque de RF. Es notable la reducción del tiempo de diseño cuando se aplica la metodología, ya que son pocos los ajustes necesarios posteriores a la elección del punto de diseño, un hecho que se ha probado en los circuitos diseñados mediante simulación eléctrica e implementación experimental.

- Se ha demostrado la utilidad de la herramienta g_m/I_D en el diseño RF, al cubrir sistemáticamente todas las regiones de inversión del transistor MOS explotando todo el potencial del transistor MOS y los compromisos entre las especificaciones de comportamiento del bloque de RF.

- Se ha validado el uso de los modelos semi-empíricos del transistor MOS basados en las características de pequeña señal de este dispositivo: la razón transconductancia a corriente de drenador, g_m/I_D, frente a la corriente normalizada i, la conductancia g_{ds}, las cinco capacidades del modelo cuasi-estático y los parámetros de ruido.

- El límite cuasi-estático de un décimo de la frecuencia de transición, usado para reducir el número de capacidades involucradas y para simplificar el estudio del transistor MOS, ha mostrado ser válido en los diseños considerados. Los resultados también son aceptables cuando se trabaja un poco más allá de este límite.

- Se ha probado la validez de los modelos simplificados de los dispositivos pasivos de RF, obtenidos a través de simulaciones AC para las frecuencias de trabajo asumidas.

- El modelado del transistor MOS y de los elementos pasivos ha sido muy eficiente pues los datos recogidos son reutilizados en todos los circuitos y flujos de diseño.

- Se ha mostrado que para los circuitos de RF implementados, integrados en tecnologías nanométricas, los mejores compromisos de funcionamiento generalmente ocurren en la región de inversión moderada del transistor MOS. Las medidas realizadas sobre los diseños implementados y los valores derivados de los flujos de diseño alcanzan una buena concordancia.

- Se han desarrollado metodologías de diseño específicas para las arquitecturas de LNAs y LC-VCOs.

  Se ha considerado el ruido de drenador y el ruido de flicker de los transistores MOS para todas las regiones de inversión.

- En el LC-VCO, han sido estudiados los compromisos de diseño dados por la región de inversión y el valor de la inductancia del tanque. Se ha visto como diseñar en inversión moderada/débil lleva a una reducción en el consumo y a un incremento en el ruido de fase. Por otra parte, reducir el valor del inductor del tanque contribuye a una mejora en la pureza espectral del VCO.

  Se ha presentado un modelo de ruido de fase del LC-VCO, basado en el modelo de Hajimiri, para todas las regiones de inversión del transistor MOS.

- El estudio de performance del LNA ha sido hecho variando el nivel de inversión y la corriente del drenador del transistor MOS. Se han demostrado buenos compromisos cuando se trabaja en inversión moderada/débil en términos de ruido y ganancia.

  La expresión de la figura de ruido del LNA ha sido ampliada incluyendo el ruido flicker del transistor MOS.

  Se ha desarrollado un estudio de los efectos de segundo orden de la resistencia de polarización a la entrada del LNA.

7.2 Líneas futuras

- Validar con circuitos fabricados la metodología de diseño del CG-LNA esbozada al final del Capítulo 4.
- Usar la metodología en circuitos complejos como LNAs de dos etapas o PAs multi-etapa.
- Estudiar la viabilidad de usar el esquema de diseño para frecuencias más altas, incluyendo los efectos no-cuasiestáticos del transistor MOS, en caso de ser necesarios.
- Incluir un modelo de los parásitos del layout en la metodología de diseño, dado que en el caso del LNA su funcionamiento se degrada cuando el esquemático es trasladado al layout.
- Utilizar el diseño final obtenido con las rutinas de cálculo que implementan los flujos de diseño como puntos de partida para herramientas de optimización automática.
- Intentar implementar un modelo semi-empírico del transistor MOS basado en las expresiones analíticas de los modelos EKV o ACM.

Bibliography

[Acos 02] R. Acosta, F. Silveira, and P. Aguirre. "Experiences on analog circuit technology migration and reuse". In: *Proceedings of 15th Symposium on Integrated Circuits and Systems Design*, pp. 169 – 174, 2002.

[Agui 03] P. Aguirre and F. Silveira. "Design of a reusable rail-to-rail operational amplifier". In: *Proceedings of 16th Symposium on Integrated Circuits and Systems Design, 2003*, pp. 20 – 25, 2003.

[Agui 08] P. Aguirre and F. Silveira. "CMOS op-amp power optimization in all regions of inversion using geometric programming". In: B. Gramado, Ed., *Proceedings of the 21st Symposium on Integrated Circuits and System Design, SBCCI*, pp. 152–157, Sep. 2008.

[Amer 07] A. Amer, E. Hegazi, and H. F. Ragaie. "A 90-nm Wideband Merged CMOS LNA and Mixer Exploiting Noise Cancellation". *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 2, pp. 323–328, 2007.

[Andr 01] P. Andreani and H. Sjöland. "Noise Optimization of an Inductively Degenerated CMOS Low Noise Amplifier". *IEEE Transactions on Circuits and Systems*, Vol. 48, No. 9, pp. 835–841, Sept 2001.

[Andr 91] A. Andreou, K. Boahen, P. Pouliquen, A. Pavasovic, R. Jenkins, and K. Strohbehn. "Current-mode subthreshold MOS circuits for analog VLSI neural systems". *IEEE Transactions on Neural Networks*, Vol. 2, No. 2, pp. 205 –213, March 1991.

[Arna 03] A. Arnaud and C. Galup-Montoro. "Pico-A/V range CMOS transconductors using series-parallel current division". *Electronic Letters*, Vol. 39, No. 18, pp. 1295–1296, Sep. 2003.

[Arna 04] A. Arnaud and C. Galup-Montoro. "Consistent noise models for analysis and design of CMOS circuits". *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, Vol. 51, No. 10, pp. 1909–1915, 2004.

[Arna 06] A. Arnaud, R. Fiorelli, and C. Galup-Montoro. "Nanowatt, Sub-nS OTAs, With Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors". *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 9, pp. 2009–2018, 2006.

[Bara 10] N. Barabino, R. Fiorelli, and F. Silveira. "Efficiency Based Design for Fully-Integrated Class C RF Power Amplifiers in Nanometric CMOS". In: F. Paris, Ed., *IEEE International Symposium in Circuits and Systems, ISCAS 2010. Proceedings*, May 2010.

[Barb 06] L. Barboni, R. Fiorelli, and F. Silveira. "A tool for design exploration and power optimization of CMOS RF circuit blocks". *IEEE International Symposium on Circuits and Systems ISCAS'06*, May 2006.

[Barr 11a] M. J. Barragán, R. Fiorelli, G. Leger, A. Rueda, and J. L. Huertas. "Alternate Test of LNAs Through Ensemble Learning of On-Chip Digital Envelope Signatures". *Journal of Electronic Testing: Theory and Applications*, Vol. 27, pp. 277–288, June 2011.

[Barr 11b] M. J. Barragán, R. Fiorelli, G. Leger, A. Rueda, and J. L. Huertas. "Improving the accuracy of RF alternate test using multi-VDD conditions: application to envelope-based test of LNAs". In: *20th Asian Test Symposium, ATS'11*, november 2011.

[Beff 02] F. Beffa *et al.* "A 6.5-mW receiver front-end for Bluetooth in 0.18-μm CMOS". In: *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp*, pp. 391–394, 2002.

[Belo 06] L. Belostotski and J. W. Haslett. "Noise Figure Optimization of Inductively Degenerated CMOS LNAs With Integrated Gate Inductors". *IEEE Transactions on Circuits and Systems*, Vol. 53, No. 7, pp. 1409–1422, Jul 2006.

[Belo 08] L. Belostotski and J. Haslett. "Two-port noise figure optimization of source-degenerated cascode CMOS LNAs". *Analog Integrated Circuits and Signal Processing*, Vol. 55, pp. 125–137, 2008.

[Bend 99] C. Bender and S. Orszag. *Advanced Mathematical Methods for Scientists and Engineers I, Asymptotic Methods and Perturbation Theory*. Springer, 1999.

[Bink 08] D. Binkley. *Tradeoffs and Optimization in Analog CMOS Design*. John Wiley and Sons, 2008.

[BSIM 08] BSIM Research Group. "BSIM3v3 and BSIM4 MOS Model". 2008. www-device.eecs.berkeley.edu/ bsim3/bsim4.html.

[Cast 85] R. Castello and P. Gray. "A high-performance micropower switched-capacitor filter". *IEEE Journal of Solid-State Circuits*, Vol. 20, No. 6, pp. 1122 – 1132, Dec. 1985.

[Cha 09] J. Cha, W. Woo, C. Cho, Y. Park, C.-H. Lee, H. Kim, and J. Laskar. "A highly-linear radio-frequency envelope detector for multi-standard operation". In: *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, pp. 149 –152, june 2009.

[Chan 06] C.-Y. Chan, J.-D. Jin, Y.-S. Lin, S. S. H. Hsu, and Y.-Z. Juane. "STI Effect on Flicker Noise in 0.13μm RF NMOS". In: *Proceeding of the 36th European Solid-State Device Research Conf. ESSDERC 2006*, pp. 101–104, 2006.

[Chen 08] W.-H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad. "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation". *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 5, pp. 1164–1176, 2008.

[Cunh 98] A. Cunha, M. Schneider, and C. Galup-Montoro. "An MOS transistor model for analog circuit design". *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 10, pp. 1510–1519, Oct. 1998.

[De R 02] C. De Ranter, G. Van der Plas, M. Steyaert, G. Gielen, and W. Sansen. "CYCLONE: automated design and layout of RF LC-oscillators". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 21, No. 10, pp. 1161 – 1170, Oct. 2002.

[Deng 11] Z. Deng and A. M. Niknejad. "On the Noise Optimization of CMOS Common-Source Low-Noise Amplifiers". *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, Vol. 58, No. 4, pp. 654–667, 2011.

[DJCo 04] D.J.Comer and D. Comer. "Using the weak inversion region to optimize input stage design of CMOS op amps". *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 51, No. 1, pp. 8 – 14, jan 2004.

[Do 08] A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, and A. Cabuk. "A Subthreshold Low-Noise Amplifier Optimized for Ultra-Low-Power Applications in the ISM Band". *IEEE Transactions on Microwave Theory and Techniques*, Vol. 56, No. 2, pp. 286–292, Feb. 2008.

[Do 09] A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, and A. Cabuk. "A Weak-Inversion Low-Power Active Mixer for 2.4 GHz ISM Band Applications". *IEEE Microwave and Wireless Components Letters*, Vol. 19, No. 11, pp. 719–721, Nov. 2009.

[Do 10] A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, and A. Cabuk. "An Energy-Aware CMOS Receiver Front End for Low-Power 2.4-GHz Applications". *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, Vol. 57, No. 10, pp. 2675–2684, Oct. 2010.

[Enz 06] C. Enz and E. Vittoz. *Charge-based MOS transistor modeling*. John Wiley and Sons, 2006.

[Fior 08a] R. Fiorelli and F. Silveira. "Common gate LNA design space exploration in all inversion regions". In: *Argentine School of Micro-Nanoelectronics, Technology and Applications, EAMTA*, pp. 119 – 122, Sep. 2008.

[Fior 08b] R. Fiorelli, F. Silveira, E. Peralías, D. Vázquez, A. Rueda, and J. L. Huertas. "A 2.4GHz LNA in a 90-nm CMOS Technology Designed with ACM Model". In: *Proceedings of the 21th Symposium on Integrated Circuits and Systems Design (SBCCI)*, ACM, Gramado, Brazil, Set 2008.

[Fior 09] R. Fiorelli, E. Peralías, and F. Silveira. "Phase noise - Consumption Trade-off in Low Power RF-LC-VCO Design in Micro and Nanometric Technologies". In: *Proceedings of the 22th Symposium on Integrated Circuits and Systems Design (SBCCI)*, ACM, Natal, Brazil, Set 2009.

[Fior 10] R. Fiorelli, E. Peralías, N. Barabino, and F. Silveira. "A fully differential monolithic 2.4GHz PA for IEEE 802.15.4 based on efficiency design flow". In: *17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, pp. 603 –606, Dec. 2010.

[Fior 11a] R. Fiorelli, E. Peralías, and F. Silveira. "LC-VCO design optimization methodology based on the g_m/I_D ratio for nanometer CMOS technologies". *IEEE Transactions on Microwave Theory and Techniques*, Vol. 59, No. 7, pp. 1822–1831, July 2011.

[Fior 11b] R. Fiorelli, F. Silveira, and E. Peralías. "Noise Figure - Power Consumption Optimization Methodology for CS-LNA based on g_m/I_D for All-Inversion-Regions". *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, 2011. under revision.

[Fior 11c] R. Fiorelli, A. Villegas, E. Peralías, D. Vázquez, and A. Rueda. "2.4-GHz single-ended input low-power low-voltage active front-end for

ZigBee applications in 90nm CMOS". In: *Proceedings of 20th European Conference on Circuit Theory and Design, ECCTD*, pp. 858–861, Aug. 2011.

[Fior 12] R. Fiorelli, E. Peralías, and F. Silveira. "An all-inversion-region g_m/I_D based design methodology for radiofrequency blocks in CMOS nanometer technologies". In: G. Cornetta, D. Santos, and J. Vazquez, Eds., *Wireless Radio-Frequency Standards and System Design: Advanced Techniques*, IGI Global, 2012.

[Flan 97] D. Flandre, A. Viviani, J.-P. Eggermont, B. Gentinne, and P. G. A. Jespers. "Improved Synthesis of Gain-Boosted Regulated-Cascode CMOS Stages Using Symbolic Analysis and g_m/I_D Methodology". *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 7, pp. 1006–1012, July 1997.

[Galu 05] C. Galup-Montoro, M. C. Schneider, H. Klimach, and A. Arnaud. "A compact model of MOSFET mismatch for circuit design". *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 8, pp. 1649–1657, 2005.

[Galu 07] C. Galup-Montoro and M. Schneider. *MOSFET Modeling for Circuit Analysis and Design*. World Scientific, 2007.

[Galu 99] C. Galup-Montoro, M. C. Schneider, and A. A. Cunha. "A Current-Based MOSFET Model for Integrated Circuit Design". In: E. Sánchez-Sinencio and A. Andreou, Eds., *Low Voltage/Low Power Integrated Circuits and Systems*, Chap. 2, pp. 7–55, IEEE Press, Piscataway, NJ, 1999.

[Geor 05] J. Georgiou and C. Toumazou. "A 126-μW cochlear chip for a totally implantable system". *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 2, pp. 430 – 443, Feb. 2005.

[Gild 06] G. Gildenblat, X. Li, W.Wu, H. Wang, A. Jha, R. van Langevelde, G. Smit, A. Scholten, and D. Klaassen. "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation". *IEEE Transactions on Electron Devices*, Vol. 53, No. 9, pp. 1979–1993, Sep. 2006.

[Gira 06] A. Girardi and S. Bampi. "Power constrained design optimization of analog circuits based on physical g_m/I_D characteristics". In: M. G. Brasil, Ed., *Proceedings of the 19th Symposium on Integrated Circuits and System Design (SBCCI)*, Aug. 2006.

[Haji 02] A. Hajimiri. *Trade-offs in Analog Circuit Design*, Chap. Trade offs in oscillator phase noise, pp. 551–585. Kluwer Academic Publishers, 2002.

[Haji 98] A. Hajimiri and T. Lee. "A general theory of phase noise in electrical oscillators". *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 2, pp. 179–194, Feb. 1998.

[Haji 99] A. Hajimiri and T. H. Lee. "Design Issues in CMOS Differential LC Oscillators". *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 5, pp. 717–724, 1999.

[Ham 01] D. Ham and A. Hajimiri. "Concepts and methods in optimization of integrated LC VCOs". *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 6, pp. 896 –909, June 2001.

[Ham 02] D. Ham. *Trade-offs in Analog Circuit Design*, Chap. Design of integrated LC-VCOs, pp. 517–549. Kluwer Academic Publishers, 2002.

[Harr 03] R. Harrison and C. Charles. "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications". *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 6, pp. 958–965, June 2003.

[He 03] J. He, X. Xi, M. Bucher, F. Krummenacher, and P. Faran. "An advanced surface potential-plus MOSFET model". In: *Proc. Workshop on Compact Modeling, Nanotech'03*, pp. 262–265, 2003.

[Hega 03] E. Hegazi and A. A. Abidi. "Varactor characteristics, oscillator tuning curves, and AM-FM conversion". *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 6, pp. 1033–1039, 2003.

[Heim 95] P. Heim and M. Jabri. "MOS cascode-mirror biasing circuit operating at any current level with minimal output saturation voltage". *Electronics Letters*, Vol. 31, No. 9, pp. 690 –691, Apr. 1995.

[Isma 03] A. Ismail and A. Abidi. "CMOS differential LC oscillator with suppressed up-converted flicker noise". In: *Digest of Technical Papers of the IEEE International Solid-State Circuits Conference, ISSCC*, IEEE, Feb 2003.

[ITRS 09] ITRS. "ITRS Roadmap 2009 System Drivers". 2009. http://www.itrs.net/Links/2009ITRS/Home2009.htm.

[Jans 02] J. Janssens and M. Steyaert. *CMOS Celular Receiver Front-ends*. Kluwer Academic Publishers, 2002.

[Jarv 05] J. A. M. Jarvinen, J. Kaukovuori, J. Ryynanen, J. Jussila, K. Kivekas, M. Honkanen, and K. A. I. Halonen. "2.4-GHz receiver for sensor applications". *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 7, pp. 1426–1433, 2005.

[Jesp 10] P. G. Jespers. *The g_m/I_D Methodology, a sizing tool for low-voltage analog CMOS Circuits*. Springer, 2010.

[Jhon 09] H.-S. Jhon, H. Jung, M. Koo, I. Song, and H. Shin. "0.7 V Supply Highly Linear Subthreshold Low-Noise Amplifier Design for 2.4GHz Wireless Sensor Network Applications". *Microwave And Optical Technology Letters*, Vol. 51, No. 5, pp. 1316–1320, May 2009.

[Jia 05] L. Jia, J.-G. Ma, K. S. Yeo, and M. A. Do. "A novel methodology for the design of LC tank VCO with low phase noise". In: *IEEE International Symposium on Circuits and Systems, ISCAS*, pp. 376 – 379 Vol. 1, May 2005.

[Joo 09] S. Joo, T.-Y. Choi, and B. Jung. "A 2.4-GHz Resistive Feedback LNA in 0.13μ CMOS". *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 11, pp. 3019–3029, 2009.

[Kao 05] Y.-H. Kao and M.-T. Hsu. "Theoretical analysis of low phase noise design of CMOS VCO". *IEEE Microwave and Wireless Components Letters*, Vol. 15, No. 1, pp. 33 – 35, Jan. 2005.

[Klum 04] E. A. M. Klumperink, S. M. Louwsma, G. J. M. Wienk, and B. Nauta. "A CMOS switched transconductor mixer". *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 8, pp. 1231–1240, 2004.

[Koom 73] J. Koomen. "Investigation of the MOST channel conductance in weak inversion". *Solid-State Electronics*, Vol. 16, No. 7, pp. 801 – 810, 1973.

[Kwon 05] I. Kwon and K. Lee. "An integrated low power highly linear 2.4-GHz CMOS receiver front-end based on current amplification and mixing.". *IEEE Microwave and Wireless Components Letters*, Vol. 15, pp. 36–38, Jan. 2005.

[Le 09] V. H. Le, S.-K. Han, J.-S. Lee, and S.-G. Lee. "Current-Reused Ultra Low Power, Low Noise LNA+Mixer". *IEEE Microwave and Wireless Components Letters*, Vol. 19, No. 11, pp. 755–757, 2009.

[Lee 00] T. H. Lee and A. Hajimiri. "Oscillator phase noise: a tutorial". *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 3, pp. 326–336, 2000.

[Lee 04] T. H. Lee. *The design of CMOS radio-frequency integrated circuits.* Cambridge University Press, second Ed., 2004.

[Lee 06] H. Lee and S. Mohammadi. "A 3GHz subthreshold CMOS low noise amplifier". In: *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006.

[Lee 07] H. Lee and S. Mohammadi. "A subthreshold Low Phase Noise CMOS LC VCO for ultra low power applications". *IEEE Microwave and Wireless Component Letters*, Vol. 17, No. 11, pp. 796–799, Nov. 2007.

[Leen 01] D. Leenaerts, J. van der Tang, and C. S. Vaucher. *Circuit Design for RF Transceivers*. Springer, 1st Ed., 2001.

[Lees 66] D. Leeson. "A Simple Model of Feedback Oscillator Noise Spectrum". *Proceedings of the IEEE*, Vol. 54, pp. 329–330, Feb. 1966.

[Leun 08] L. L. K. Leung and H. C. Luong. "A 1 V 9.7 mW CMOS Frequency Synthesizer for IEEE 802.11a Transceivers". *IEEE Transactions on Microwave Theory and Techniques*, Vol. 56, No. 1, pp. 39–48, Jan. 2008.

[Lina 03] B. Linares-Barranco and T. Serrano-Gotarredona. "On the design and characterization of femtoampere current-mode circuits". *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 8, pp. 1353 – 1363, aug. 2003.

[Lisc 05] A. Liscidini, M. Brandolini, D. Sanzogni, and R. Castello. "A 0.13 μm CMOS front-end for DCS1800/UMTS/802.11b-g with multi-band positive feedback low noise amplifier". In: *Proc. Digest of Technical Papers VLSI Circuits 2005 Symp*, pp. 406–409, 2005.

[Lisc 06] A. Liscidini, A. Mazzanti, R. Tonietto, L. Vandi, P. Andreani, and R. Castello. "Single-Stage Low-Power Quadrature RF Receiver Front-End: The LMV Cell". *IEEE Journal of Solid-State Circuits*, Vol. 41, No. 12, pp. 2832–2841, 2006.

[Lu 06] Y. Lu, K. S. Yeo, A. Cabuk, J. Ma, M. A. Do, and Z. Lu. "A novel CMOS low-noise amplifier design for 3.1- to 10.6-GHz ultra-wide-band wireless receivers". *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, Vol. 53, No. 8, pp. 1683–1692, Aug. 2006.

[Malo 95] F. Maloberti, F. Francesconi, P. Malcovati, and O. Nys. "Design considerations on low-voltage low-power data converters". *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 42, No. 11, pp. 853 –863, Nov. 1995.

[Mang 06] M. Manghisoni, L. Ratti, V. Re, V. Speziali, and G. Traversi. "Noise Characterization of 130nm and 90nm CMOS Technologies for Analog Front-end Electronics". In: *2006 IEEE Nuclear Science Symposium Conference Record.*, pp. 214–218, 2006.

[Mell 01] T. Melly, A.-S. Porret, C. C. Enz, and E. A. Vittoz. "An Ultralow -Power UHF Transceiver Integrated in a Standard Digital CMOS Process: Transmitter". *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 3, pp. 467–472, March 2001.

[Mell 11] D. Mellouli, D. Cordeau, J. Paillot, H. Mnif, and M. Loulou. "Graphical method for the phase noise optimization applied to a 6-GHz fully integrated NMOS differential LC VCO". In: *IEEE 9th International New Circuits and Systems Conference (NEWCAS)*, pp. 85 –88, June 2011.

[Miur 96] M. Miura-Mattausch, U. Feldmann, A. Rahm, M. Bollu, and D. Savignac. "Unified complete MOSFET model for analysis of digital and analog circuits". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 1, pp. 1–7, 1996.

[Nguy 04] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, , and S.-G. Lee. "CMOS Low-Noise Amplifier Design Optimization Techniques". *IEEE Transactions on Microwave Theory and Techniques*, Vol. 52, No. 5, pp. 1433–1442, May 2004.

[Nguy 10] T.-K. Nguyen, H. Kang, N.-S. Kim, , and C.-S. Pyo. "A Low-Power CMOS Dual-Band RF Receiver for IEEE 802.15.4-Based Sensor Node Applications". *Microwave and Optical Technology Letters*, Vol. 51, No. 1, pp. 163–166, Jan 2010.

[Nieu 09] A. Nieuwoudt, T. Ragheb, H. Nejati, and Y. Massoud. "Numerical Design Optimization Methodology for Wideband and Multi-Band Inductively Degenerated Cascode CMOS Low Noise Amplifiers". *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, Vol. 56, No. 6, pp. 1088–1101, 2009.

[Nikn 00] A. M. Niknejad. "Analyis of Si Inductors and Transformers for IC's (ASITIC)". 2000. http://rfic.eecs.berkeley.edu/ niknejad/asitic.html.

[O 02] K. K. O, N. Park, and D.-J. Yang. "1/f noise of NMOS and PMOS transistors and their implications to design of voltage controlled oscillators". In: *Proc. of IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 59–62, 2002.

[Oh 05] N.-J. Oh and S.-G. Lee. "Building a 2.4-GHz radio transceiver using IEEE 802.15.4". 2005. Circuits and Devices Magazine, IEEE.

[Park 08] K.-G. Park, C.-Y. Jeong, J.-W. Park, J.-W. Lee, J.-G. Jo, , and C. Yoo. "Current Reusing VCO and Divide-by-Two Frequency Divider for Quadrature LO Generation". *IEEE Microwave and Wireless Components Letters*, Vol. 18, No. 6, pp. 413–415, June 2008.

[Peru 08] B. Perumana, S. Chakraborty, C.-H. Lee, and J. Laskar. "A Low-Power Fully Monolithic Subthreshold CMOS Receiver With Integrated LO Generation for 2.4 GHz Wireless PAN Applications". *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 10, pp. 2229–2238, Oct 2008.

[Porr 01] A.-S. Porret, T. Melly, D. Python, C. C. Enz, and E. A. Vittoz. "An Ultralow -Power UHF Transceiver Integrated in a Standard Digital CMOS Process: Arquitecture and Receiver". *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 3, pp. 452–464, March 2001.

[Ramo 04] J. Ramos, A. Mercha, W. Jeamsaksiri, D. Linten, S. Jenei, R. Rooyackers, R. Verbeeck, S. Thijs, A. J. Scholten, P. Wambacq, I. Debusschere, and S. Decoutere. "90nm RF CMOS technology for low-power 900MHz applications". *Proceeding of the 34th European Solid-State Device Research conference ESSDERC 2004*, pp. 329–332, Sep. 2004.

[Ramo 05] J. Ramos, K. Francken, G. Gielen, and M. Steyaert. "An Efficient, Fully Parasitic-Aware Power Amplifier Design Optimization Tool". *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 52, No. 8, pp. 1526 – 1534, aug. 2005.

[Rodr 04] E. Rodriguez-Villegas, A. Yufera, and A. Rueda. "A 1.25-V micropower Gm-C filter based on FGMOS transistors operating in weak inversion". *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 1, pp. 100 – 111, Jan. 2004.

[Rofo 96] A. Rofougaran, J.-C. Chang, M. Rofougaran, and A. Abidi. "A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver". *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 7, pp. 880 –889, July 1996.

[Sanc 10] C. Sánchez-López, R. Castro-López, E. Roca, F. Fernández, R. Gonzalez-Echevarría, J. Esteban-Muller, J. López-Villegas, J. Sieiro, and N. Vidal. "A bottom-up approach to the systematic design of LNAs using evolutionary optimization". In: *2010 XIth International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design (SM2ACD)*, pp. 1 –5, Oct. 2010.

[Scho 04] A. Scholten, L. Tiemeijer, R. van Langevelde, R. Havens, A. Z. van Duijnhoven, R. de Kort, and D. Klaassen. "Compact modelling of noise for RF CMOS circuit design". *IEE Proceedings Circuits Devices Systems*, Vol. 151, No. 2, 2004.

[Sens 09] B. Sensale, R. Fiorelli, and F. Silveira. "Common Source LNA Design Space Exploration in All Inversion Regions". In: *XV Iberchip Workshop*, March 2009.

[Shae 97] D. Shaeffer and T. H. Lee. "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier". *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 5, pp. 745–759, May 1997.

[Sham 06] A. Shameli and P. Heydari. "A novel power optimization technique for ultra-low power RFIDs". In: Tegernsee-Germany, Ed., *International Symposium on Low Power Electronics and Design*, 2006.

[Shen 08] J. Shen and P. Kinget. "A 0.5-V 8-bit 10-Ms/s Pipelined ADC in 90-nm CMOS". *IEEE Journal of Solid-State Circuits*, Vol. 43, No. 4, pp. 787 –795, Apr. 2008.

[Shi 09] J. Shi, Y. Z. Xiong, , K. Kang, L. Nan, and F. Lin. "RF Noise of 65-nm MOSFETs in the Weak-to-Moderate-Inversion Region". *IEEE Electron Device Letters*, Vol. 30, No. 2, pp. 185–188, Feb. 2009.

[Silv 00] F. Silveira and D. Flandre. "Analysis and design of a family of low-power class AB operational amplifiers". In: *Proceedings of 13th Symposium on Integrated Circuits and Systems Design*, pp. 94 –98, 2000.

[Silv 04] F. Silveira and D. Flandre. *Low Power Analog CMOS for Cardiac Pacemakers. Design and Optimization in Bulk and SOI Technologies*. The Kluwer International Series in Engineering and Computer Science, 2004.

[Silv 96] F. Silveira, D. Flandre, and P. G. A. Jespers. "A g_m/I_D based methodology for the design of CMOS analog circuits and its applications to the synthesis of a silicon-on-insulator micropower OTA". *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 9, pp. 1314–1319, Sep. 1996.

[Sivo 05] P. Sivonen and A. Parssinen. "Analysis and optimization of packaged inductively degenerated common-source low-noise amplifiers with ESD protection". *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 4, pp. 1304–1313, 2005.

[Song 06] T. Song, H.-S. Oh, S. Hong, and E. Yoon. "A 2.4-GHz sub-mW CMOS receiver front-end for wireless sensors network". *IEEE Microwave and Wireless Components Letters*, Vol. 16, pp. 206–208, 2006.

[Tang 08] L.-F. Tanguay and M. Sawan. "An ultra-low power ISM-band integer-N frequency synthesizer dedicated to implantable medical microsystem". *Analog Integrated Circuit and Signal Processing*, Vol. 58, No. 3, pp. 205–214, March 2008.

[Tsiv 00] Y. Tsividis. *Operation and Modelling of the MOS Transistor*. Oxford University Press, 2nd Ed., 2000.

[Tzen 08] F. Tzeng, A. Jahanian, and P. Heydari. "A Multiband Inductor-Reuse CMOS Low-Noise Amplifier". *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, Vol. 55, No. 3, pp. 209–213, 2008.

[Vald 08] A. Valdés-García, R. Venkatasubramanian, J. Silva-Martinez, and E. Sánchez-Sinencio. "A Broadband CMOS Amplitude Detector for On-Chip RF Measurements". *IEEE Transactions on Instrumentation and Measurement*, Vol. 57, No. 7, pp. 1470 –1477, July 2008.

[Vill 07] A. Villegas. *Modelado de un receptor ZigBee - IEEE 802.15.4. Diseño del mezclador y del filtro de canal en tecnología CMOS*. Master's thesis, Universidad de Sevilla-España, 2007.

[Vill 10] A. Villegas, D. Vazquez, and A. Rueda. "A low power low voltage mixer for 2.4 GHz applications in CMOS-90nm technology". *Design and Diagnostics of Electronic Circuits and Systems, DDECS*, pp. 44–47, 2010.

[Vitt 77] E. Vittoz and J. Fellrath. "CMOS analog integrated circuits based on weak inversion operations". *IEEE Journal of Solid-State Circuits*, Vol. 12, No. 3, pp. 224 – 231, June 1977.

[Vitt 79] E. Vittoz and O. Neyroud. "A low-voltage CMOS bandgap reference". *IEEE Journal of Solid-State Circuits*, Vol. 14, No. 3, pp. 573 – 579, June 1979.

[Vitt 85] E. Vittoz. "The Design of High-Performance Analog Circuits on Digital CMOS Chips". *IEEE Journal of Solid-State Circuits*, Vol. 20, No. 3, pp. 657 – 665, June 1985.

[VPCD 09] VPCD. "Virtuoso Passive Component Designer". 2009. http://www.cadence.com.

[Wata 99] G. Watanabe and H. Lau. "CMOS RF buffer amplifier design". In: *Asia Pacific Microwave Conference*, pp. 230 –233 vol.2, nov 1999.

[Wu 98] S. Wu and B. Razavi. "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications". *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 12, pp. 2178 –2185, Dec. 1998.

[Xuan 10] K. Xuan, K. F. Tsang, W. C. Lee, and S. C. Lee. "0.18 μm CMOS dual-band low-noise amplifier for ZigBee development". *Electronics Letters*, Vol. 46, No. 1, pp. 85–86, 2010.

[Yufe 05] A. Yufera, A. Rueda, J. Muñoz, R. Doldan, G. Leger, and E. Rodriguez-Villegas. "A tissue impedance measurement chip for myocardial ischemia detection". *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 52, No. 12, pp. 2620 – 2628, Dec. 2005.

[Zhuo 05] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sánchez-Sinencio. "A capacitor cross-coupled common-gate low-noise amplifier". *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, Vol. 52, No. 12, pp. 875–879, 2005.

[Ziel 86] V. der Ziel. *Noise in Solid State Devices and Circuits*. Wiley, 1986.

[Zito 09] D. Zito. "A novel low-power receiver topology for RF and microwave applications". *International Journal of Circuit Theory and Applications*, Vol. 37, pp. 1008–1018, Nov. 2009.

List of Symbols and Acronyms

List of symbols

Symbol	Description
A_i	MOS intrinsic gain
C_{MOS}	VCO cross-coupled MOS capacitance
C_{cap}	Capacitor equivalent capacitance
C_{var}	Varactor equivalent capacitance
$C_{bde(bse)}$	MOS extrinsic bulk-source capacitance
$C_{d1(d2)}$	LNA output network capacitances
C_{gde}	MOS extrinsic gate-drain capacitance
C_{gse}	MOS extrinsic gate-source capacitance
C_{ext}	LNA external capacitor
C_{load}	VCO load capacitance
C_{tank}	VCO tank resistance
C_{ij}	MOS intrinsic capacitance
CG_V	Conversion Gain (Volts)
C_{ox}	MOS normalized oxide capacitance
C_t	LNA gate-source equivalent capacitance
c	Correlation coefficient
F	Noise factor
F_C	Critical longitudinal field
f_c	MOS transistor corner frequency
$f_{c,1/f^3}$	flicker corner frequency
f_0	Working frequency
f_T	MOS transition frequency
fng	Varactor number of fingers
G	LNA power gain
G_{eff}	LNA equivalent transconductance
g_{ds}	MOS drain-source conductance
g_{ds}/I_D	MOS conductance to current ratio
g_{d0}	g_{ds} at zero drain-source voltage
g_{ind}	Inductor parallel conductance
g_m	MOS transconductance
g_m/I_D	MOS transconductance to current ratio
g_{ms}	MOS source transconductance
g_{tank}	VCO tank conductance
g_{var}	Varactor parallel conductance
grp	Group of fingers of the varactor
H_b	LNA R_{bias} noise transfer function
I_F	MOS channel forward current
I_D	MOS drain current

Symbol	Description
I_R	MOS channel reverse current
I_S	MOS specific current
$IIP2$	Input second order intermodulation point
$IIP3$	Input third order intermodulation point
i	MOS normalized current
i_F	MOS channel normalized forward current
i_R	MOS channel normalized reverse current
$\overline{i_d^2}$	MOS drain noise psd
$\overline{i_g^2}$	MOS induced gate noise psd
$\overline{i_{w,d}^2}$	MOS channel white noise psd
$\overline{i_{1/f,d}^2}$	MOS flicker noise psd
K_F	Flicker noise constant
k_B	Boltzmann constant $k_B = 1.3806 \times 10^{-23} JK^{-1}$
k_{osc}	oscillation factor
k_0	VCO general flicker corner constant
L	MOS channel length
$L_{(.)}$	LNA inductance
L_{ind}	Inductor equivalent inductance
$hg(lg)$	LNA high/low gain mode
$\mathcal{L}$	VCO phase noise
NF	LNA noise figure
n	Slope factor
n_f	MOS number of fingers
$P_{av,(.)}$	Available power in a circuit element
$P_{carrier}$	VCO carrier power
$P_{harm}^{2^{nd}}$	second order harmonic power
$P_{harm}^{3^{rd}}$	third order harmonic power
$P_{sideband}$	VCO single sideband power at Δf
$P1dB$	1-dB compression point
P_{out}	Output power
P_{NW}	Delivered power to PA NW
q_{max}	VCO tank capacitance charge
Q_{tank}	VCO tank quality factor
Q_L	LNA input network quality factor
$Q_{(.)}$	Component quality factor
R	$R_s - R_g$
R_s	LNA source impedance

Symbol	Description
R_{ext}	LNA input biasing blocking resistance
R_{NW}	PA resistance seen from the drain MOS
R_g	LNA gate equivalent resistance
R_L	LNA load resistance
R_{lim}	LNA minimum parallel resistance of L_s
$R_{p,(.)}$	Component parasitic parallel resistance
R_{res}	Resistor equivalent resistance
$R_{s,(.)}$	Component parasitic serial resistance
$R_\square$	MOS gate sheet resistance
S_{ij}	S-parameters
T	absolute temperature
U_T	Thermal voltage
V_{DD}	Supply voltage
V_P	Pinch-off voltage
V_{OD}	Overdrive voltage
V_T	Threshold voltage
V_{out}	VCO output voltage amplitude
V_{gs}	MOS gate-source voltage
v_s	Input voltage source
v_{sat}	MOS carrier velocity saturation
W	MOS channel length
W_n	MOS channel finger length
$Y_L^{'}$	LNA input admittance of the output stage
Z_{in}	LNA input impedance
$Z_{o,MOS}$	LNA core output impedance
$\Lambda_{(.)}^{(s/p)}$	LUT of the serial/parallel component model
α	$\alpha = g_m/g_{d0}$
α_{lin}	linearity error
Δ	LNA drain noise transfer function
Δ_f	VCO frequency offset from the carrier
δ	Gate noise coefficient
ε_0	Vacuum permitivity
ε_{Si}	Silicon relative permitivity
Γ	LNA gate noise transfer function
Γ_{ISF}	Impulse sensitivity function
γ	Excess noise factor
$\gamma_B^{(\ /')}$	body effect coefficient for long/short channel MOS
μ	Effective mobility
η	PA power efficiency
η_{MOS}	PA MOST power efficiency
η_{NW}	PA NW power efficiency
ϕ	VCO arbitrary phase

Abbreviations

Acronyms	Description
ACM	MOST advanced compact model
BSIM	analytical compact model
BIST	built-in self-test
CG − LNA	common gate LNA
CS − LNA	common source LNA
EKV	MOST analytical compact model
ESD	electrostatic discharge
FoM	figure of merit
LNA	low noise amplifier
LC − VCO	inductor-capacitor VCO
LUT	look-up table
MI	MOST moderate inversion
MIM	metal-insulator-metal
MOST	metal-oxide-semiconductor field-effect transistor
NW	matching network
OQPSK	Offset Quadrature PSK
PA	power amplifier
psd	power spectral density
RF	radiofrequency
SI	MOST strong inversion
SW − MIX	switched transconductor mixer
*TECH*1(2)	CMOS technology utilized
VCO	voltage controlled oscillator
WI	MOST weak inversion